SENECA: Flexible and Scalable Neuromorphic Processor
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SENECA

SENECA (Scalable Energy-efficient NEuromorphic Computer Architecture) [1] is a RISC-V-based digital neuromorphic processor targeting extreme edge and near-sensor applications:

- **Energy-Efficient** event-driven computation exploits activation sparsity in edge neural networks.
- **Low-Latency** parallel processing via single-core SIMD and multi-core asynchronous execution.
- **On-device Adaptation** enables privacy-aware learning and increases robustness in deployment.

Comparison with State-of-the-art Neuromorphic Designs

SENECA improves state-of-the-art neuromorphic designs in following aspects:

- **Flexible** programmable neural models, synaptic models and learning algorithms.
- **Area-Efficient** 3-level memory hierarchy allows novel embedded memory technologies.
- **Multi-Precision** graded spikes, weights, and neural states in 3 data types: int4, int8, BF16.
- **Core-to-Core Asynchronous Parallelism** without global synchronization overhead.
- **End-to-End Application Deployment** with pre/post and main network processing in one go.

SENECA Architecture

- **Novel hierarchical control system** consists of RISC-V and Loop Buffer guarantees flexibility and efficiency at the same time.
- **Neuron Processing Element array** (NPE) accelerates neural network computation.
- **Network-on-Chip** (NOC) with multicasting, compression mechanism, source-based routing.
- **Customizable and scalable digital IP** on number of cores, NPE array size, memory size, targeting a wide range of applications.

Comparison of SENECA with SpiNNaker2

- **End application deployment** to pre/post and main network processing in one go.
- **Minimum overhead** with global synchronization.
- **Core programmability** for models and learning algorithms.
- **Novel hierarchical control system** improves state of the art of neuromorphic designs.

Comparison of SENECA with SpiNNaker2

- **Memory-efficient processing** via weight and state reuse for high-resolution event cameras.
- **Minimum overhead** on pre- and post-processing benefit from our novel hierarchical control system.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Energy/SOp (pJ)</th>
<th>Area (mm²/Core)</th>
<th>Memory (Mb/Core)</th>
<th>Flexibility</th>
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</table>

Table 1. Neuromorphic state-of-the-art comparison

 SpiNNaker2

- **Latency** 1x
- **Energy/SOp** (pJ) 2.7

Table 2. Event-driven processing optimization

- **Binary Spike**
- **_low_ precision**
- **_spike-grouping**
- **Binary Spike**
- **Graded Spike**

- **Latency**
- **Energy/SOp** (pJ)

Figure 1. Single-core (top) and 64-core (bottom) SENECA architecture

Figure 2. Event-driven processing and spike grouping optimization

Figure 3. Event-driven convolutional layer processing

On-device Adaptation and Learning

- **On-device adaptation** for sensor aging, domain shifting, new class adding, via few-shot learning and continual learning.

Figure 4. Online recurrent learning of e-prop (from [Bellec et al., 2020])

Collaboration and Contact

SENECA platform is accessible for academic research and welcome industrial collaboration, please contact us!

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Publications


Acknowledgement

This technology is partially funded and initiated by the Netherlands and European Union’s Horizon 2020 research and innovation projects TEMPO (ECSEL Joint Undertaking under grant agreement No 869252), ANDANTE (ECSEL Joint Undertaking under grant agreement No 876925), DAIS (Key Digital Technologies Joint Undertaking under grant agreement No 10107223) and REBECCA (Key Digital Technologies Joint Undertaking under grant agreement No 10107224).