Image Sensors For Low Power Applications

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3/22/2021
1. Introduction to image sensors
2. Image sensor architecture vs. power efficiency
3. Image sensors for computer vision
4. Trade-off between power and performance
5. Power reduction techniques from a user’s perspective
6. Ultra-low power HDR Digital Pixel Sensor from FRL
1. **Introduction to image sensors**
2. Image sensor architecture vs. power efficiency
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INTRODUCTION TO IMAGE SENSORS

Charge Coupled Device (CCD) Image Sensor

Willard Boyle & George Smith 2009 Nobel Prize

Michael Tompsett

1969
CCD Invention

1971
1st CCD Image Sensor

@ Bell Labs
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Scientific Applications:
Space telescope, biological imaging

Consumer products:
Digital camera, camcorder in 90s, 00s
INTRODUCTION TO IMAGE SENSORS

CMOS Image Sensor (CIS)

1960s
MOS Image Sensor
Pioneering work

Peter Noble
Gene Weckler
INTRODUCTION TO IMAGE SENSORS

CMOS Image Sensor (CIS)

Peter Noble  Gene Weckler  Eric Fossum

1960s MOS Image Sensor Pioneering work

1993 CIS Invention @ JPL

Founded Photobit in 1995
INTRODUCTION TO IMAGE SENSORS

CMOS Image Sensor (CIS)

- Peter Noble: MOS Image Sensor Pioneering work in the 1960s
- Gene Weckler: MOS Image Sensor Pioneering work in the 1960s
- Eric Fossum: CIS Invention in 1993 at JPL
- Founded Photobit in 1995
- 2000: 1st camera phone sold by Sharp
- 2007: iPhone 1st gen
- 2010: iPhone 4
- 2017: iPhone X

- 2007: 1st generation iPhone
- 2010: iPhone 4
- 2017: iPhone X

Timeline:
- 1960s: MOS Image Sensor Pioneering work
- 1993: CIS Invention
- 2000: 1st camera phone sold by Sharp
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2000 1st camera phone sold by Sharp

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2017 iPhone X

2019 Oculus Quest
Signal Flow in An Image Sensor

Light → Electron → Voltage → Digital Numbers
Signal Flow in An Image Sensor

1. Light
2. Photodetector
3. Electron
4. Capacitor and amplifier
5. Voltage
6. ADC
7. Digital numbers
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Pixel Array

- An image sensor contains a 2-D array of photodetectors
- One fundamental aspect of image sensor design is how to read out signals from a pixel array, and power efficiency depends on the chosen scheme
- At least two peripheral circuit blocks needed
  - Driver to address pixels
  - “Serializer” to send pixel data off-chip one by one
Pixel Array Readout Process in CCD Image Sensor

- Shifting pixel data in charge domain
- Extremely high charge transfer efficiency required
- High voltage driver, large pixel capacitance to drive every shift, special fabrication process which prevents signal processing blocks like ADC to be integrated
- Not power efficient
Pixel Array Readout Process in CMOS Image Sensor

- Each pixel contains a source follower to convert signal to voltage domain
- Pixel output becomes addressable in voltage domain through analog switches and column buses
- Pixel driver can be implemented with CMOS logic
- Additional signal processing circuits including ADCs can be integrated on the same chip
- Generally more power efficient than CCD image sensor
Driving Column Bus in Voltage Domain

- Each pixel source follower need to drive parasitic resistors and capacitors from other pixels on the same column bus
- Typical parameters
  - VAA: 2.5~3.0V
  - SF W/L ratio: ~1
  - Column bias current: 1~10uA
  - Settling time: 1~10us
  - Parasitic cap per pixel: ~10fF
  - Consume both static and dynamic current
Digital Pixel Sensor (DPS)

- Each pixel contains an ADC to covert pixel signal to digital numbers and pixel memory for storage
- Pixel data is readout in digital domain
- Additional pixel driving signals needed to drive ADC in each pixel
- Ultra-low power DPS from FRL to be introduced later
Power Efficiency Advantage of Digital Pixel Sensor (DPS)

- At architecture level
  - Each pixel source follower only drives an in-pixel ADC, no parasitics from column bus
  - Reading out pixel data in digital domain is more power efficient than reading out in voltage domain
  - All ADCs are operated at the same time after exposure which allows power-gating peripheral supporting circuitry for ADC, like reference generator, ramp generator, digital blocks and PLL, outside of the short ADC operating period

- More power efficient than traditional CIS

<table>
<thead>
<tr>
<th>Power related parameters in pixel array readout process (typical values)</th>
<th>CIS (Voltage)</th>
<th>DPS (Digital)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.5~3.0V</td>
<td>1.2V or lower</td>
</tr>
<tr>
<td>Static current</td>
<td>1~10uA</td>
<td>No</td>
</tr>
<tr>
<td>Bus parasitic capacitance</td>
<td>~10fF x No. of rows</td>
<td>~1fF x No. of rows x No. of memory cells per pixel</td>
</tr>
<tr>
<td>Settling time</td>
<td>1~10us</td>
<td>10~100ns</td>
</tr>
<tr>
<td>Benefit from process scaling</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Image Sensor Architecture vs. Power Efficiency

More and more power efficient in pixel array readout
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Agenda
Image Sensors Optimized For Computer Vision Algorithms

- General sensor requirements *
  - Global shutter
  - Short exposure time to minimize motion blur
  - Adequate SNR performance in low light and wide dynamic range environment
  - Low latency
  - **ultra-low power consumption to support always-on functionality in a wearable battery powered device**

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Computer Vision Use Case Example: Eye (Gaze) Tracking

- Need to capture rapid eye movement
- Using near-infrared light source to avoid visible interference to human eye
- Stringent eye safety requirement
- Cameras need to be mounted close to eyes

Sensor requirements
- Global shutter
- High frame rate up to 240 fps
- Short exposure time
- Excellent NIR sensitivity
- Small die size
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TRADE-OFF BETWEEN POWER AND PERFORMANCE

Power vs. Pixel Array Size

- Different sensor blocks scales differently with pixel array size, so total sensor power doesn’t scale linearly
- Additional pixel array parasitics need to be driven during array readout when array size increases
- Static power consumption in peripheral circuit is more efficient when shared by more pixels

![Graph showing the trade-off between energy per pixel and pixel array size. The graph indicates that as the pixel array size increases, the energy per pixel decreases to a minimum at a certain size, then increases as the parasitic effect becomes dominant.]
TRADE-OFF BETWEEN POWER AND PERFORMANCE

Power vs. Sensor Noise

- Sensor noise can be introduced at various stages in the signal flow
- Two common techniques to improve sensor noise
  - Apply gain to attenuate noise from following stages
  - Conflict with sensor dynamic range
  - Multiple sampling to reduce temporal noise
  - Higher power consumption
TRADE-OFF BETWEEN POWER AND PERFORMANCE

Power vs. Dynamic Range (Single Shot)

- Maximum signal level allowed in the signal chain defines the upper boundary of sensor dynamic range.

- Both the capacity in charge domain (full well capacity) and max voltage swing allowed are highly related to supply voltage.

- A lower supply voltage than pixel supply (VDD_PIX) is usually applied to signal chain after pixel (VDD_AMP, VDD_ADC, etc.) to reduce power.

- Photodiode is also heavily engineered to expand full well capacity without requiring higher VDD_PIX.
Power vs. High Dynamic Range

- Expanding sensor dynamic range usually requires multiple captures with either different gain or different exposure time
- Images with high gain or long exposure captures low light details
- Images with low gain or short exposure captures high light details
- Increase in power consumption is inevitable due to additional captures and the burden of synthesizing HDR images
- One way to optimize power for HDR capture is to design a pixel capable of automatically selecting gain or exposure time, like DPS from FRL
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POWER REDUCTION TECHNIQUES

Reduce Frame Rate

- Sensor power consumption is almost linearly proportional to frame rate
- Optimize algorithm to allow varying frame rate instead of constant high frame rate can help reduce sensor power significantly

Vary frame rate to reduce average frame rate
POWER REDUCTION TECHNIQUES

Subsampling/Downsampling/Region of Interest (ROI)

• All can effectively save power on data transmission between sensor and host
• Subsampling and ROI allows sensor designer the opportunity to further reduce power by only powering on and processing the needed pixels
• Downsampling implemented with charge binning on sensor can help reduce power for processing pixels, but is usually limited to 2:1
• Downsampling implemented with pixel value averaging in digital domain is less power efficient
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Pixels, ADC and memory have to be on the same process node.
3D Stacking with Pixel Parallel Connection

Pixels, ADC and memory have to be on the same process node.
3D Stacking with Pixel Parallel Connection

- Pixels and ADC+Memory can be different process nodes.

ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM FRL
ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM FRL

3D Stacking with Pixel Parallel Connection
ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM FRL*

Sensor Die Photo and Block Diagram

- 45nm/65nm stacked process
- Total pixel: 540 x 560
- Effective pixel: 512 x 512
- Die size: 4 x 4 mm

Pixel Architecture

- Pixel size 4.6um x 4.6um
- AB for global shutter
- DCG and Cs for dual conversion gain
- State latch to lock SRAM data for the corresponding ADC mode
- 10bit SRAM per pixel
Triple Quantization Scheme for HDR

- Three ADC modes
  - Low light pixel --- linear high gain PD ADC
  - Mid light pixel --- linear low gain FD ADC
  - High light pixel --- time-to-saturation TTS mode
- Sequential operation within one exposure
  - TTS during exposure
  - PD ADC
  - FD ADC
- Each pixel “automatically” selects its optimal mode for its own light level
- No gap between ADC modes
Basic 1: Charge Overflow

If PPD is full, charge will overflow to FD.
Basic 2: Charge Sensing and Conversion Gain

\[ \Delta V = \frac{Q}{C} \]

\[ C_1 \quad < \quad C_2 \]
Basic 2: Charge Sensing and Conversion Gain

\[ \Delta V = \frac{Q}{C} \]

\[ C_1 < Q_1 = C_2 = Q_2 \]
Basic 2: Charge Sensing and Conversion Gain

\[ \Delta V = \frac{Q}{C} \]

\[ \Delta V_1 \quad \Delta V_2 \]

\[ C_1 < C_2 \]
\[ Q_1 = Q_2 \]
\[ \Delta V_1 > \Delta V_2 \]
Basic 2: Charge Sensing and Conversion Gain

\[ \Delta V = \frac{Q}{C} \]

Conversion Gain (CG) : voltage swing induced by one electron on a given capacitor

\[ CG = \frac{q}{C} \text{ (μV/e-)} \]
PD ADC Phase
*(For Low Light)*
PD ADC Phase
(For Low Light)
PD ADC Phase
(For Low Light)
PD ADC Phase
(For Low Light)
PD ADC Phase
(For Low Light)
FD ADC Phase
*(For Medium Light)*
FD ADC Phase

(For Medium Light)

Potential

AB  PPD  TG  FD  LG  C_{EXT}  RST

V_{FD}
FD ADC Phase
(For Medium Light)
FD ADC Phase
(For Medium Light)
Time-To-Saturation (TTS) Phase
(For High Light)

\[ V_{TH_{TTS}} \]

\[ t \]

Not locked in TTS
Locked in TTS
ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM
FRL

Triple Quantization Scheme for HDR

Photon response curve
ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM FRL

HDR Images

Sensor output HDR image

Only showing pixels in PD ADC mode

Only showing pixels in FD ADC mode

Only showing pixels in TTS mode
ULTRA-LOW POWER HDR DIGITAL PIXEL SENSOR FROM FRL

HDR Images

Stainless mug

Filament

Letters on card

Sensor output HDR image

Only showing pixels in PD ADC mode

Only showing pixels in FD ADC mode

Only showing pixels in TTS mode
Sensor On-Chip Power Management

- Sensor operation is divided into phases with clear boundaries
- Only necessary circuit blocks are powered on at each phase

| Idle | Exposure | ADC | Send data off-chip |
## Sensor Specs Summary

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>4.6 x 4.6 um</td>
</tr>
<tr>
<td>Resolution</td>
<td>512 x 512</td>
</tr>
<tr>
<td>Technology</td>
<td>45nm/65nm stacked</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>10-bit</td>
</tr>
<tr>
<td>Read noise</td>
<td>4.2 e-</td>
</tr>
<tr>
<td>Full well (PD/FD/TTS)</td>
<td>3800e-/51000e-/9x10^6e-</td>
</tr>
<tr>
<td>FPN</td>
<td>47 e-</td>
</tr>
<tr>
<td>DR</td>
<td>127dB</td>
</tr>
<tr>
<td>QE (500nm/850nm/940nm)</td>
<td>96%/57%/40%</td>
</tr>
<tr>
<td>Power</td>
<td>5.75mW at 30fps, 3Q, 1ms exp</td>
</tr>
<tr>
<td>Max frame rate</td>
<td>480 fps</td>
</tr>
</tbody>
</table>
Low Power Image Sensors

• Fundamental power reduction requires fabrication technology advancement and innovation at architecture level

• Comprehensive on-chip power management, i.e., only power on necessary circuit blocks at each operation phase, is key to optimize image sensor power consumption

• Sensor and algorithm co-optimization, e.g., utilizing subsampling/downsampling/ROI to request only necessary data from sensor and reducing average frame rate, can push the boundary of power reduction even further
Thank you
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Along with a special thank you to the sponsors who made this event possible!
Arm: The Software and Hardware Foundation for tinyML

Connect to high-level frameworks

Profiling and debugging tooling such as Arm Keil MDK

Optimized models for embedded

Runtime (e.g. TensorFlow Lite Micro)

Optimized low-level NN libraries (i.e. CMSIS-NN)

RTOS such as Mbed OS

Arm Cortex-M CPUs and microNPUs

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Power efficiency
Model design, compression, quantization, algorithms, efficient hardware, software tool

Personalization
Continuous learning, contextual, always-on, privacy-preserved, distributed learning

Efficient learning
Robust learning through minimal data, unsupervised learning, on-device learning

Perception
Object detection, speech recognition, contextual fusion

Reasoning
Scene understanding, language understanding, behavior prediction

Action
Reinforcement learning for decision making

A platform to scale AI across the industry

Qualcomm AI Research is an initiative of Qualcomm Technologies, Inc.
Samsung brings AI in the hands of everyone, with >300M Galaxy phones per year. Fingerprint ID, speech recognition, voice assistant, machine translation, face recognition, AI camera; the application list goes on and on.

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- Edge capabilities: on-chip training, learning, and inference
- Designed for AI Edge applications: vision, audio, olfactory, and smart transducer applications
- Licensed as IP to be designed into SoC or as silicon
- Sensor inputs are analyzed at the point of acquisition rather than through transmission via the cloud to the data center. Enables real time response for power-efficient systems
- Software Development Platform
BabbleLabs AI speech wizardry in Cisco Webex

AI meets speech - deep experience in speech science, AI/ML, embedded systems

- Massive compute
  - 300 TFLOPS per engineer

- Novel deep neural networks
  - Silicon-optimized software

- Massive data corpus
  - 40K hours of speech
  - 15K hours of music
  - 10K hour of noise
  - 100K room models

- Speech enhancement
- Speech recognition

Applications:
- Conferencing
- Call centers
- Digital Assistants
- Calling
DSP Group, Inc. develops wireless communications and voice processing chipsets, algorithms, and software solutions for converged communications and smart-enabled devices. Core competencies include, but are not limited to, voice processing. Its technology supports the development and integration of voice user interfaces (VUIs) for applications ranging from smartphones to the smart home. Its Ultra-Low Energy (ULE, per the ULE Alliance) wireless solutions enable low-power, long-range, secure communication applications for the IoT and are distinguished by their native support of two-way voice communication. On-going development efforts include the application of machine learning (ML) and artificial intelligence (AI) hardware and algorithms to address the need for accurate AI solutions at the edge for applications such as sound detection, proximity detection, and acoustic beacons.
TinyML for all developers

Dataset

- Acquire valuable training data securely
- Enrich data and train ML algorithms

Test

- Embedded and edge compute deployment options
- Test impulse with real-time device data flows

Edge Device

- Real sensors in real time
- Open source SDK

www.edgeimpulse.com
The Eye in IoT
Edge AI Visual Sensors

CMOS Imaging Sensor
- Ultra Low power CMOS imager
- Ai + IR capable

IoT System on Chip
- Machine Learning edge computing silicon
- <1mW always-on power consumption
- Computer Vision hardware accelerators

Computer Vision Algorithms
- Machine Learning algorithm
- <1MB memory footprint
- Microcontrollers computing power
- Trained algorithm
- Processing of low-res images
- Human detection and other classifiers
GrAI Matter Labs has created an AI Processor for use in edge devices like drones, robots, surveillance cameras, and more that require real-time intelligent response at low power. Inspired by the biological brain, its computing architecture utilizes sparsity to enable a design which scales from tiny to large-scale machine learning applications.

www.graimatterlabs.ai
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Himax Technologies, Inc. provides semiconductor solutions specialized in computer vision. Himax’s WE-I Plus, an AI accelerator-embedded ASIC platform for ultra-low power applications, is designed to deploy CNN-based machine learning (ML) models on battery-powered AIoT devices. These end-point AI platforms can be always watching, always sensing, and always listening with on-device event recognition.

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• Guides and empowers users through the process
• Support for high accuracy applications requiring low power and small memory
• Imagimob AI have been used in 25+ tinyML customer projects
• Gesture control
Health sensors measure PPG and ECG signals critical to understanding vital signs. Signal chain products enable measuring even the most sensitive signals.

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The new MAX78000 implements AI inferences at low energy levels, enabling complex audio and video inferencing to run on small batteries. Now the edge can see and hear like never before.

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Large (3MB flash + 1MB SRAM) and small (256KB flash + 96KB SRAM, 1.6mm x 1.6mm) Cortex M4 microcontrollers enable algorithms and neural networks to run at wearable power levels.

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Advanced AI Acceleration IC

Low Power Cortex M4 Micros

Sensors and Signal Conditioning
Qeexo AutoML

Automated Machine Learning Platform that builds tinyML solutions for the Edge using sensor data

Key Features

- Supports 17 ML methods:
  - Multi-class algorithms: GBM, XGBoost, Random Forest, Logistic Regression, Gaussian Naive Bayes, Decision Tree, Polynomial SVM, RBF SVM, SVM, CNN, RNN, CRNN, ANN
  - Single-class algorithms: Local Outlier Factor, One Class SVM, One Class Random Forest, Isolation Forest
- Labels, records, validates, and visualizes time-series sensor data
- On-device inference optimized for low latency, low power consumption, and small memory footprint applications
- Supports Arm® Cortex™- M0 to M4 class MCUs

End-to-End Machine Learning Platform

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- Wearables
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- IoT
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- Explain ML models and relate the function to the physics
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https://reality.ai  info@reality.ai  @SensorAI  Reality AI
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• End-to-end AI workflow
• Multi-user auto-labeling of time-series data
• Code transparency and customization at each step in the pipeline

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Performing inference on BNNs with xcore.ai
Tuesday, March 23 at 12pm (PST)

TinyML: The power/cost conundrum
Thursday, March 25 at 12pm (PST)

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