Empowering Collaborative Chip Design: Leveraging Generative AI for Custom Accelerators and Edge AI Innovation

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efabless.com

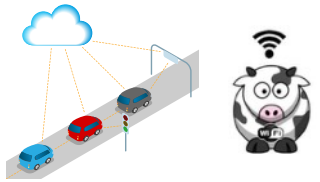
THE WORLD NEEDS CUSTOM CHIPS

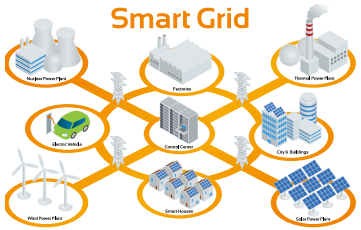
CONSUMER

Smart Home
Entertainment
Smart Recreation

INDUSTRIAL

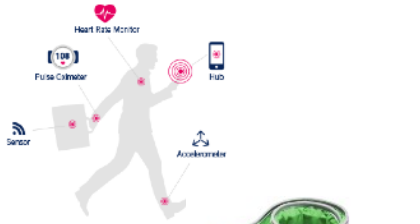
Smart Meters
Agriculture
Automotive





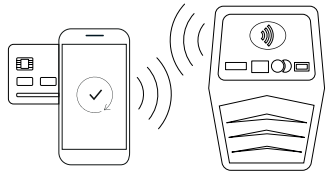
MEDICAL

Wearable Devices
Implantable Devices
Telehealth Services



RETAIL

Inventory Control
Product Tracking
Focused Marketing



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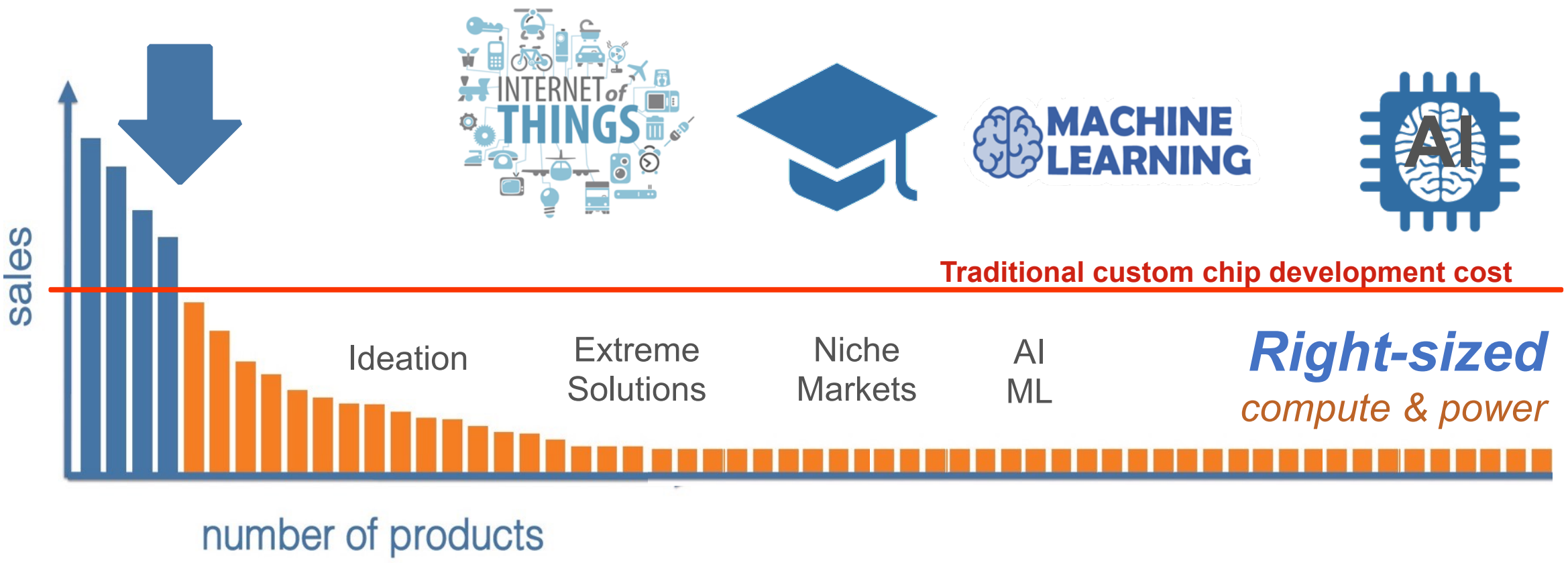
THE NEW GAME IS **CUSTOM** PRODUCTS

Long-tail Innovation is required on a massive scale to meet demand 10,000's of Products



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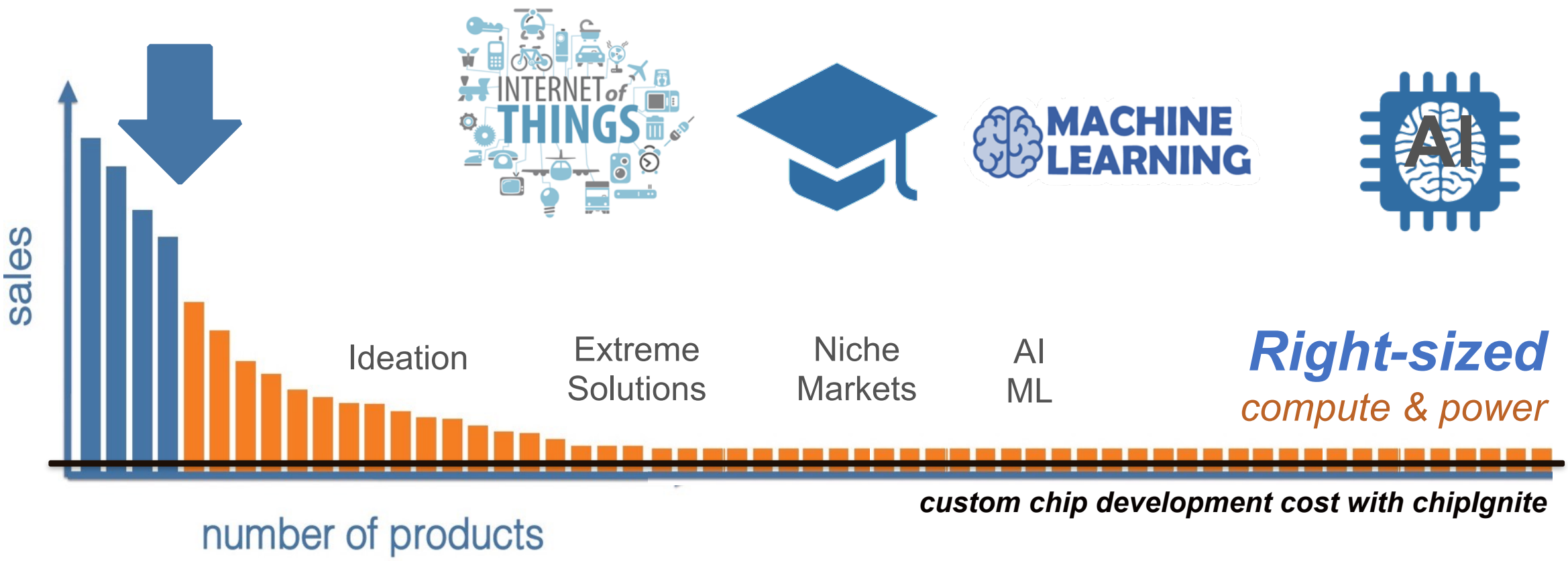

custom chip development cost with chiplgnite

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THE NEW GAME IS **CUSTOM** PRODUCTS

Right-sized

compute, power & cost

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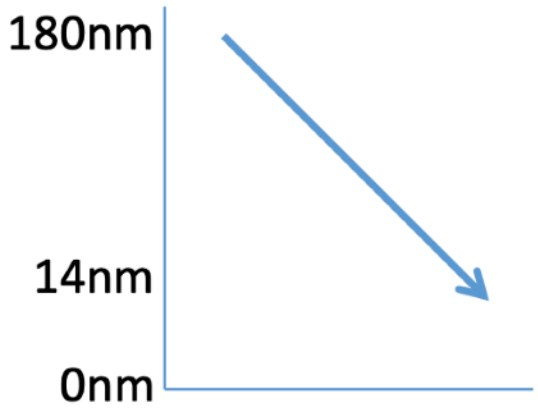
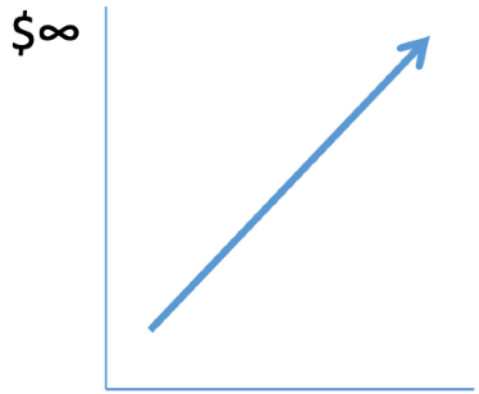
SEMICONDUCTOR INDUSTRY TRENDS

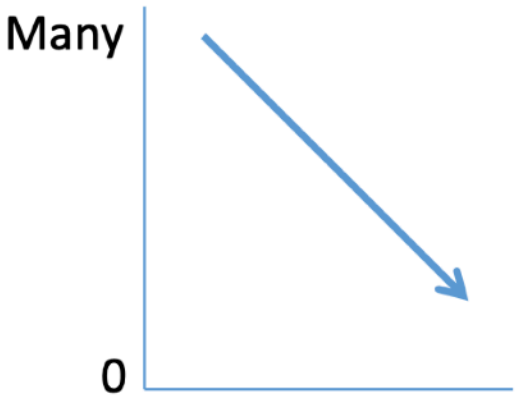
It's screaming "slow down innovation"



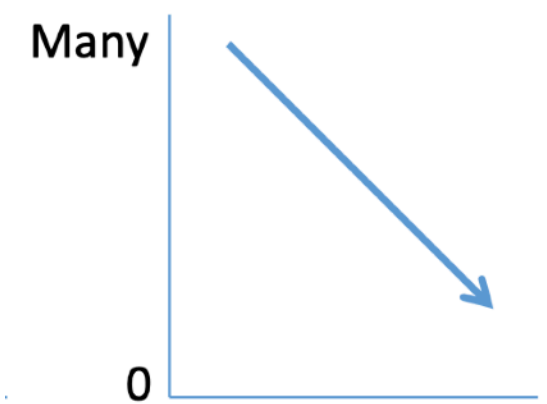
As Transistor Size Goes To Zero



Development Cost Goes to Infinity



Number of Customers Goes to Zero



Number of Designers Goes to Zero

Source: Mike Noonen

Unfortunately

Significant

Barriers Are In

The Way!

Not Enough
Chip Designers

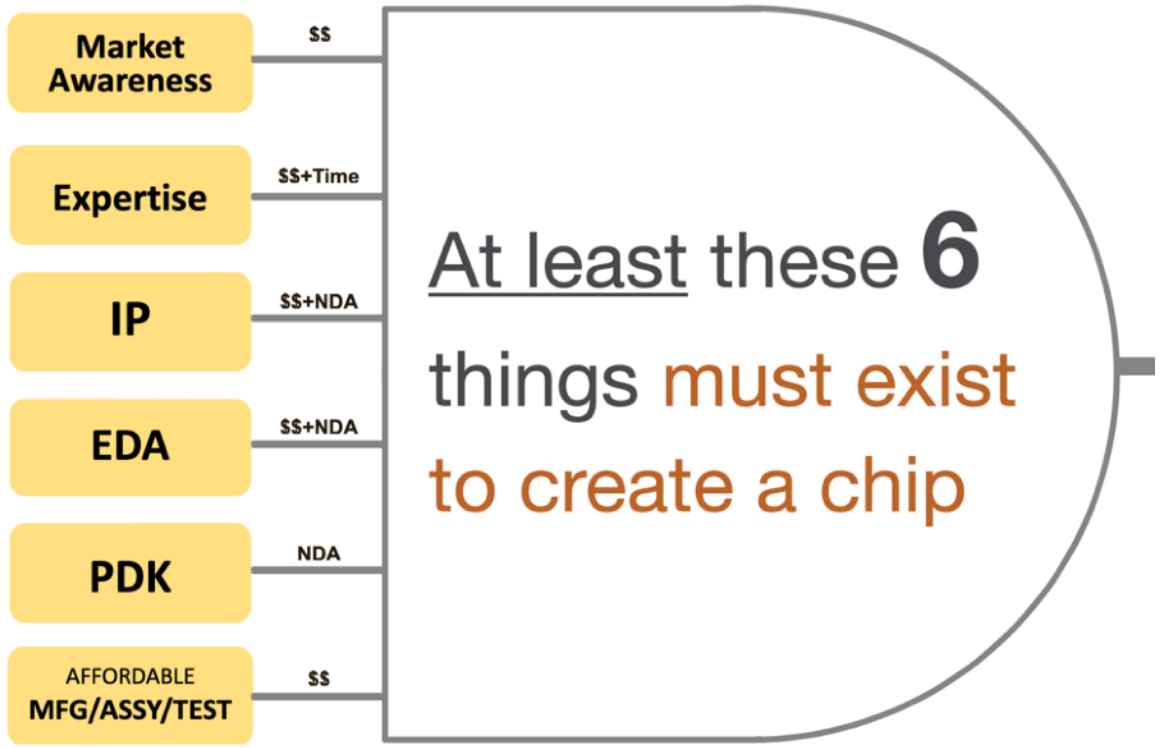
Design Costs
Too Much

And Take
Too Long

Empowering Collaborative Chip Design:

Leveraging Generative AI for Custom Accelerators and Edge AI Innovation

To simplify the process of Chip creation and make it accessible



To provide

- the business process
- the guardrails for quality
- the connection to customers
- the guardrails for IP protection
- the starting point - reference designs, IP
- the access to chip design tools flows, PDK & IP
- the scaleable & affordable cost structure

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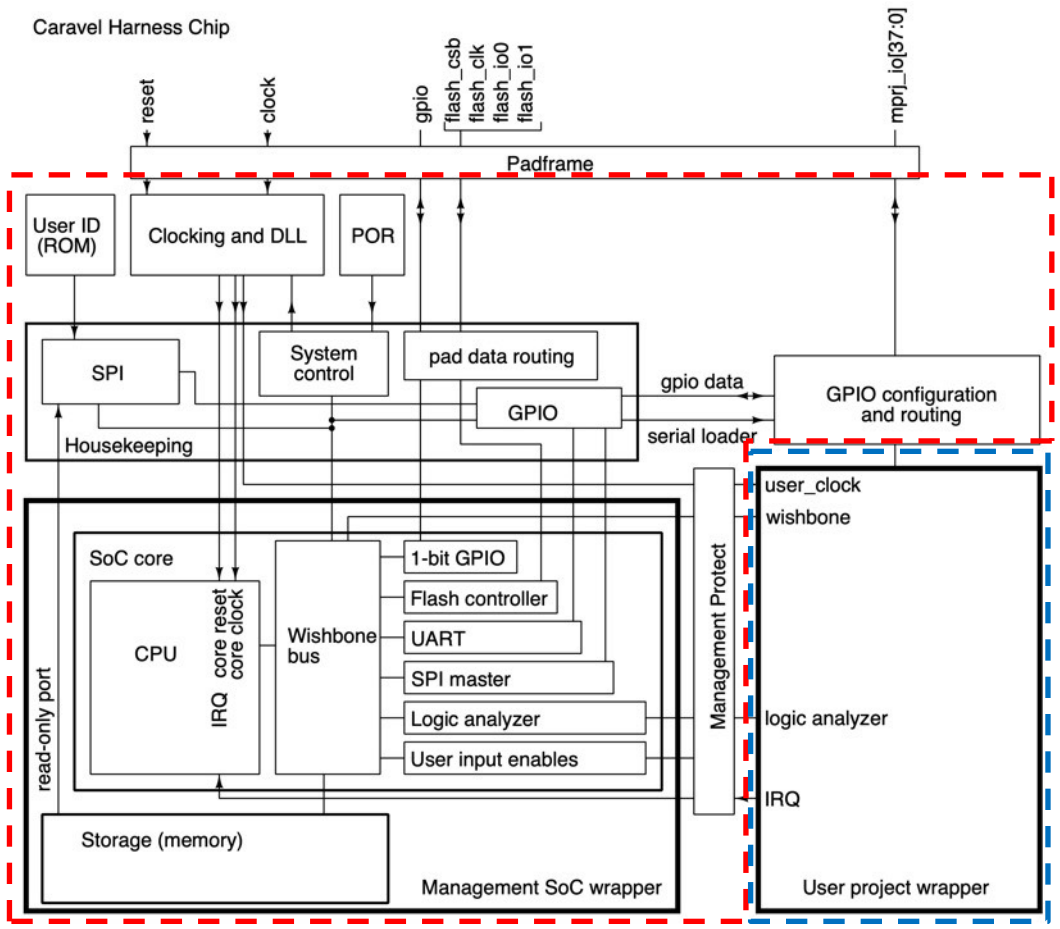
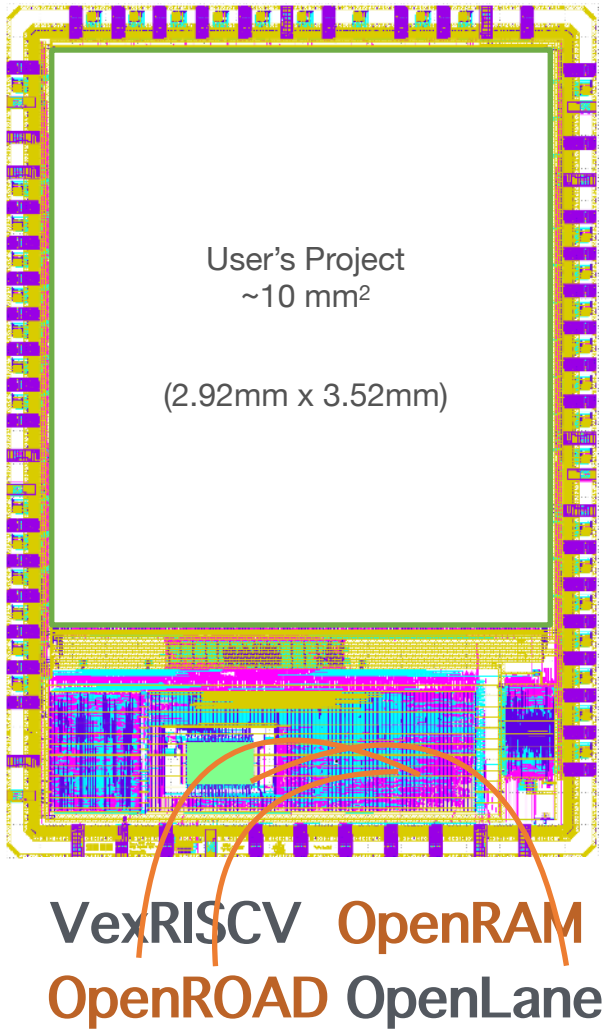
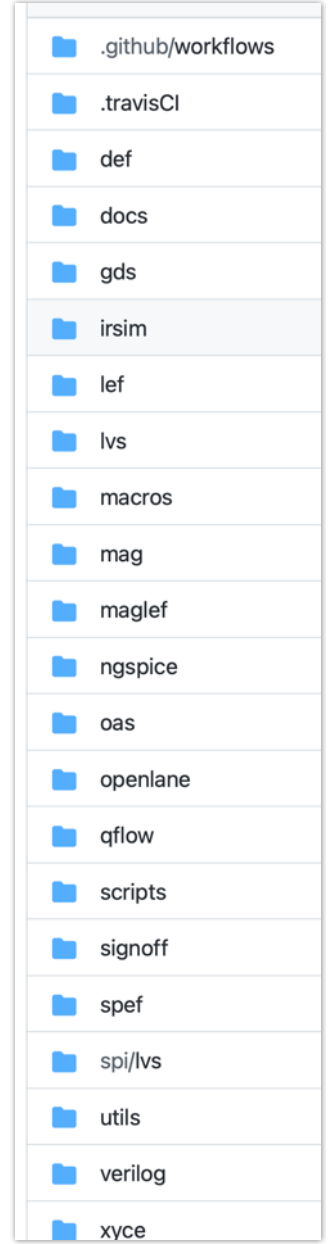
Caravel Open Source SoC Platform



https://github.com/efabless/caravel



Uniform Open Source File Structure to ease reuse & modifications



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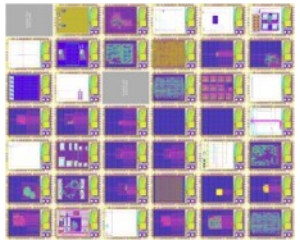


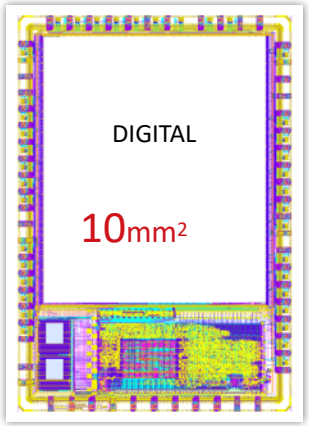
One Size Fits All

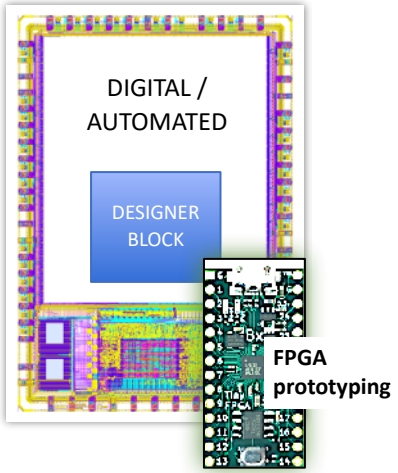
LOW COMPLEXITY

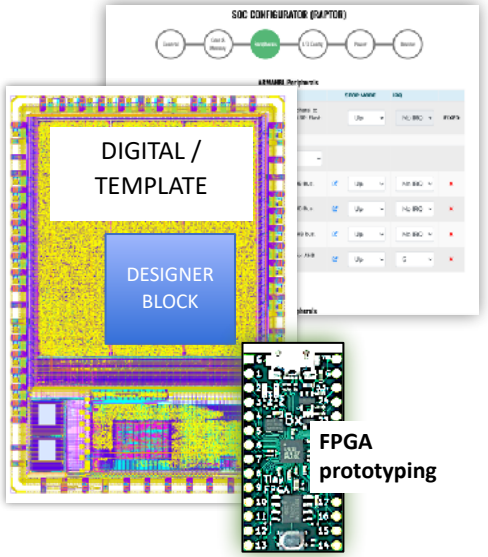
IP Development

Digital & low frequency analog

Enabling larger designer base







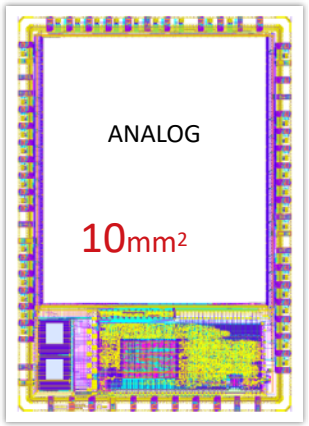
HIGH COMPLEXITY

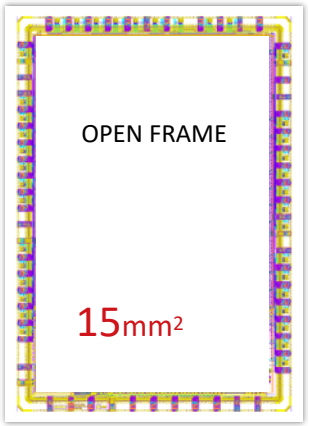
IP Development

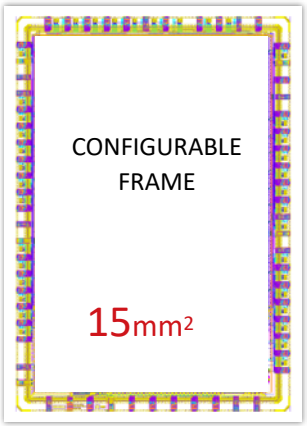
Complete Custom ASIC

Analog & Digital

Expert designer base







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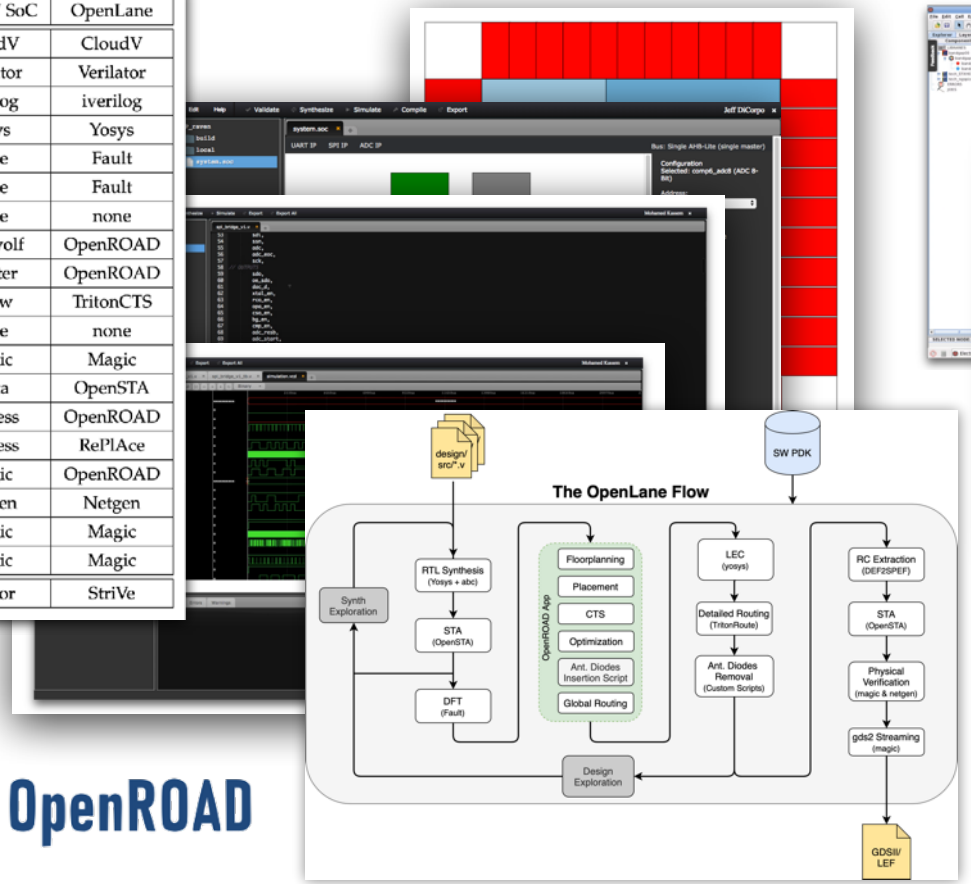
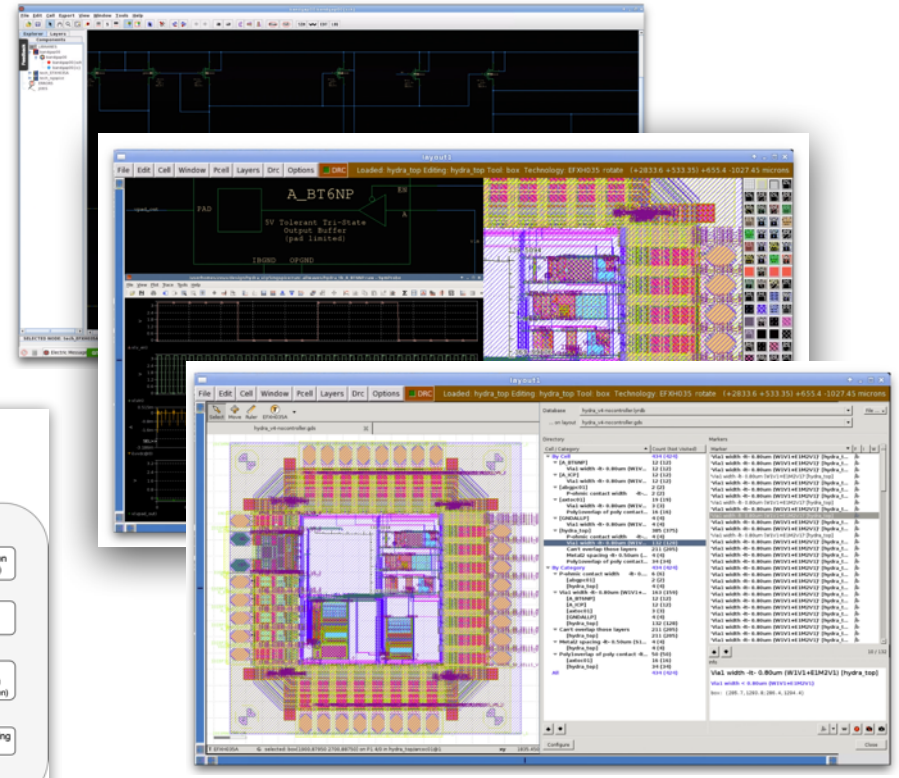
OPEN SOURCE DESIGN FLOWS

DESIGN STEP	Qflow	CloudV SoC	OpenLane
System Design	N/A	CloudV	CloudV
RTL Lint	Verilator	Verilator	Verilator
RTL Simulation	iverilog	iverilog	iverilog
Logic Synthesis	Yosys	Yosys	Yosys
DFT Scan Insertion	none	none	Fault
DFT ATPG	none	none	Fault
Formal Verification	none	none	none
Placement	graywolf	graywolf	OpenROAD
Routing	qrouter	qrouter	OpenROAD
CTS	Qflow	Qflow	TritonCTS
Dynamic EMIR	none	none	none
Extraction	Magic	Magic	Magic
Timing Analysis	Vesta	Vesta	OpenSTA
Floorplanning	Magic	efabless	OpenROAD
Top-Level Placement	Magic	efabless	RePlAce
Top-Level Routing	Magic	Magic	OpenROAD
LVS	Netgen	Netgen	Netgen
DRC	Magic	Magic	Magic
GDS	Magic	Magic	Magic
SoC	Raven	Raptor	StriVe





- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD

- Schematic Capture
- SPICE Simulation

- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification

OpenLane

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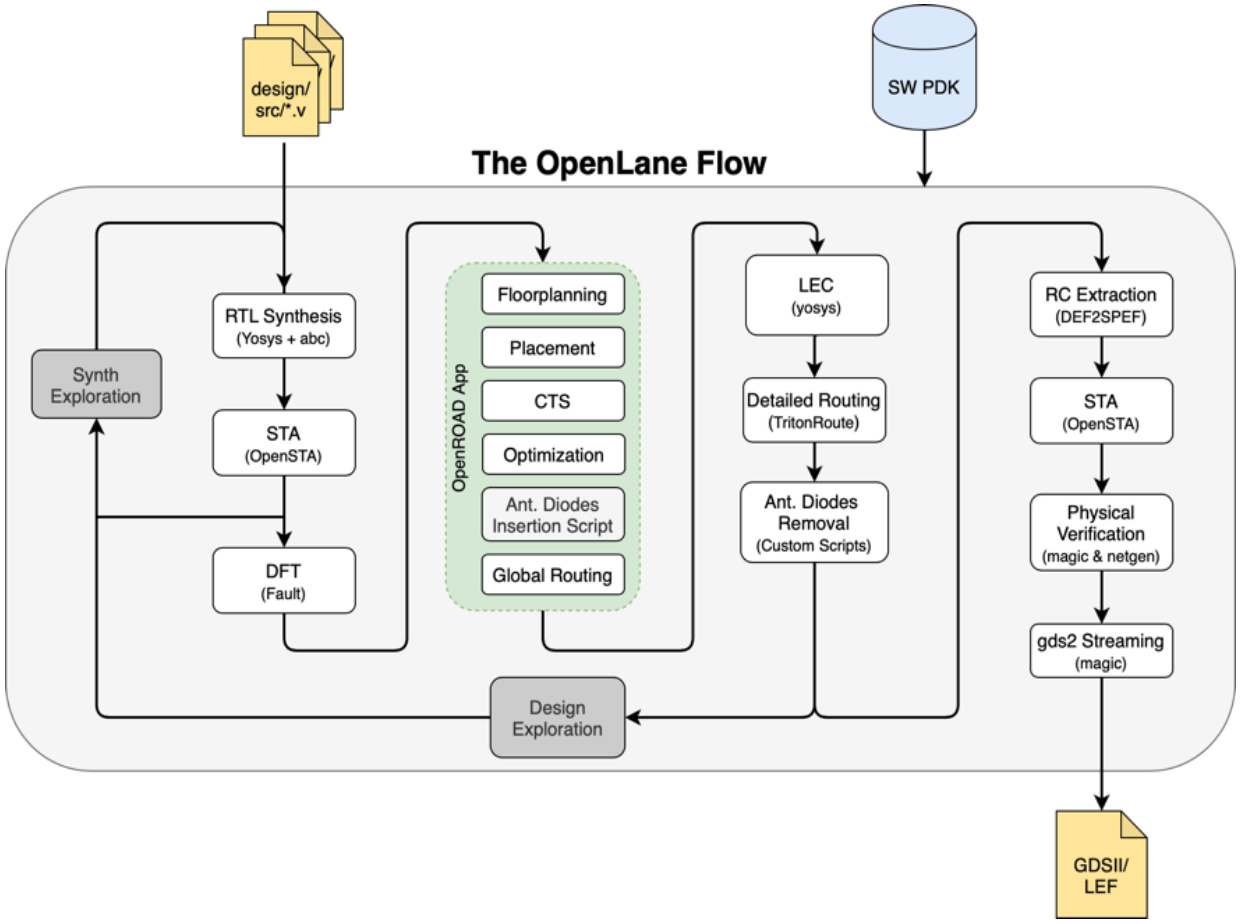
OpenLane DIGITAL COMPILER-LIKE RTL2GDS

Automate code-to-chip like a ***GNU software compiler - with trade-offs in area and performance.***

It opens the door for software developers to generate hardware That's at least a 100x more potential designers!



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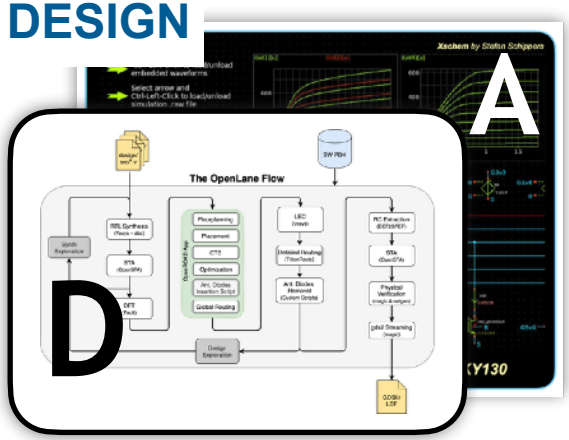
Complete & Path from Design to Test

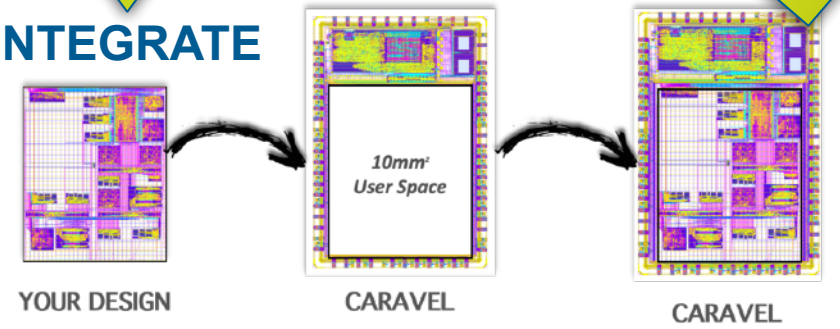
chipIgnite
Rapid IC Creation

1 DESIGN



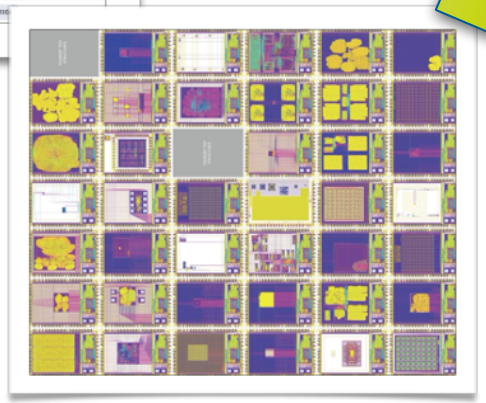
OS or Proprietary EDA Digital & Analog

2 INTEGRATE



3 SUBMIT

4 FABRICATE



5 TEST

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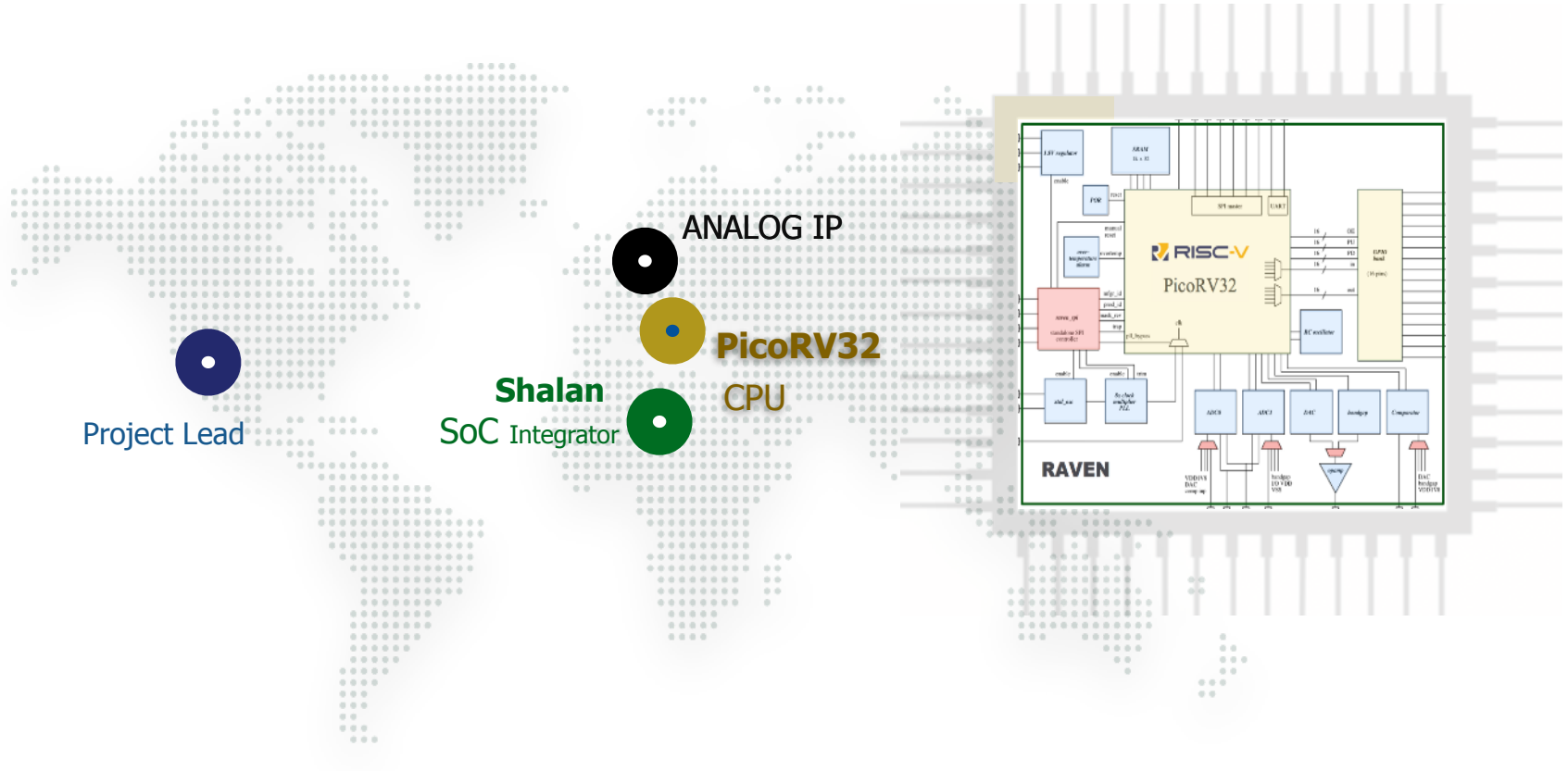
COMMUNITY COLLABORATION

- Design house or community professional to set the specs
- Collaborate with other community members to create the design
- Prototype the solutions
- Publish the design solution in the marketplace



RICH OUTCOME

COMMUNITY DEVELOPS

COMMUNITY DEFINES

Community created IP, ICs and other HW products shared, licensed and forked

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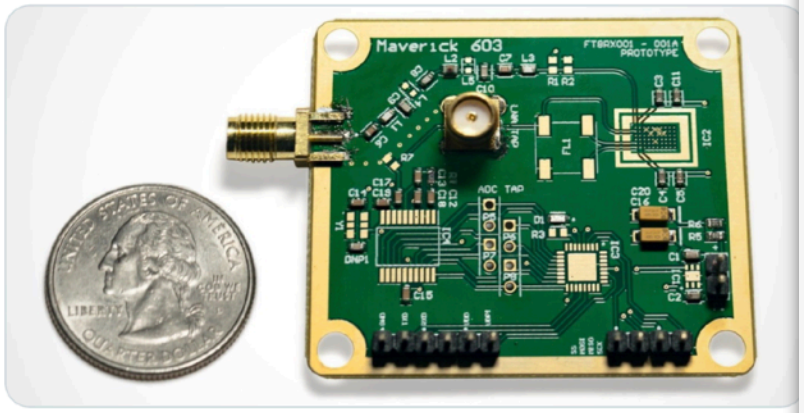
Clive (Max) Maxfield @MaxMaxfield · Jan 5

Developing the World's First Commercially Available RF Device with an Open-Source Chip eejournal.com/article/develo... It's great to see a small company use open-source tools and work with **Efabless**/SkyWater to develop a custom integrated circuit. @eetimes @MakerIO @hackaday @DesignNews



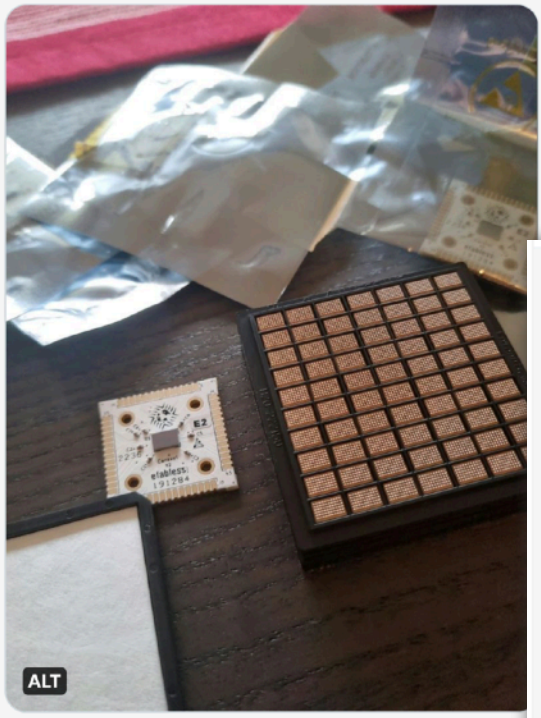
2 39 187 9,954

efabless.com @efabless · Jan 29

Glad to note that Klas Nordmark received his silicon :-) Klas an ASIC-adapted version of the award-winning bit-serial RI processor SERV.
bit.ly/3XSEJdl

github.com/klasnordmark/c...

#icdesign #asics #ASIC



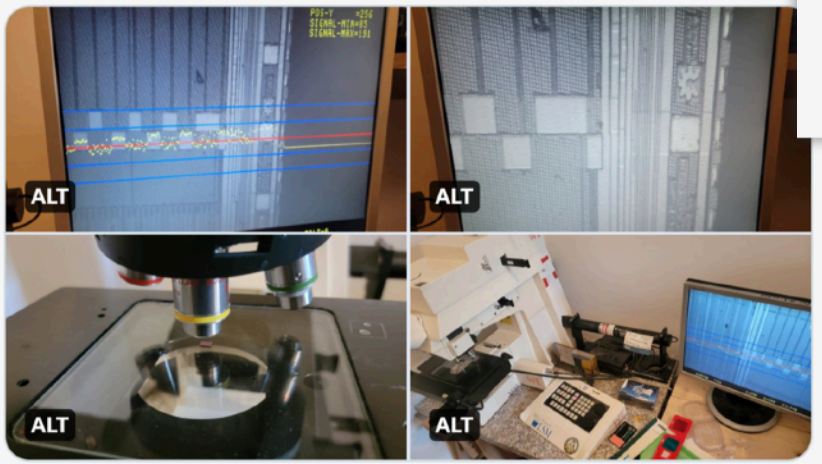
1 10 44 4,426

!WIRED Lab @ValpoWIREDlab · Apr 28, 2022

Our team's SOURCE poster about their work coming up to speed with the @OpenROAD_EDA and **@efabless** OpenMPW open source VLSI toolchain. The groundwork for switching the full chip design course to these tools.

@tucanae47 · May 1, 2022

I recently learned how to use the LSM microscope at @xHain_hackspac (super thanks to lorxor he is not on twitter) :) first images taken on my own 😱🥰 from mpw1 **efabless** dies from @matthewvenn chip that he sent to me sometime back ❤️



Michael Welling @m_w@chaos.... @QwertyEmbe... · Dec 29, 2021

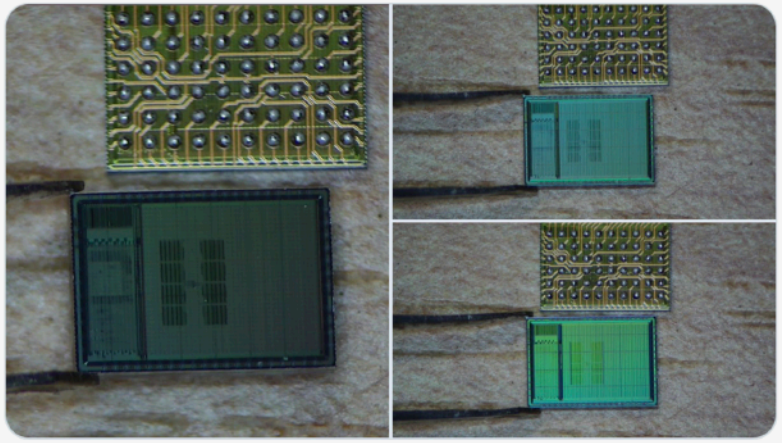
The mpw-1 versions of the PyFive caravel chips have arrived.

Here are some images courtesy of @tnt.

Thanks to **@efabless**, @SkyWaterFoundry, @Google and everyone that helped make this possible.

Hopefully we can get working silicon in the near future.

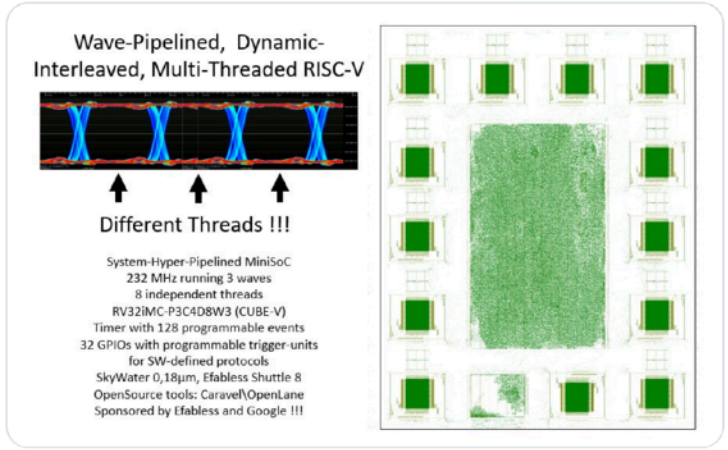
#sky130_mpw1



3 6 42

Arduissimo @arduissimo · Jan 19

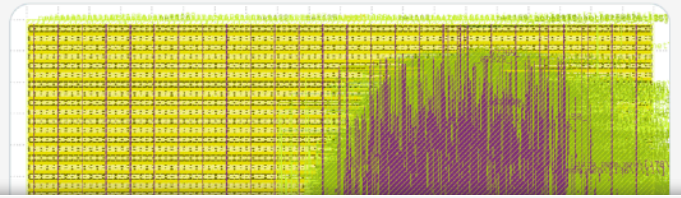
It's a TAPEOUT !!! I have been informed, that my ASIC is accepted by @Efabless (MPW-8). The CUBE-V #RISCV CPU uses WAVE-PIPELINING and dynamic-interleaved multi-threading. A 25-year-old dream comes true. Thanks @Google for sponsorship + all the many helpers on Slack @OpenROAD_EDA



8 52 310 26.6K

Johan Euphrosine @proppy · Nov 12, 2022

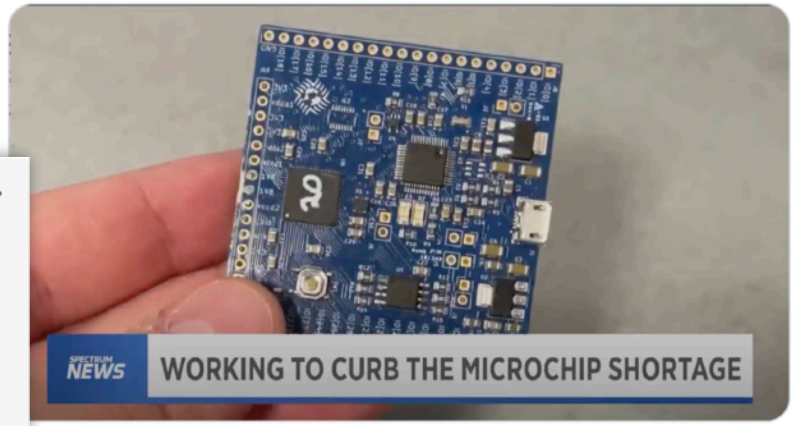
Managed to re-harden Jacaranda-8 (1st OpenMPW submission from @Cra2yPierr0t) with the @GlobalFoundries GF180MCU PDK using this @GoogleColab notebook colab.research.google.com/gist/proppy/7b...
I hope the will consider resubmitting it to @efabless's GF-MPW-0🚀:
github.com/cpu-dev/carave...



Mohamed MK @mkkassem · Jul 8, 2022

#caravel is famous ... Local News TV Star!
@NYSTEC @NYCreates #NYDESIGN @efabless #chipignite

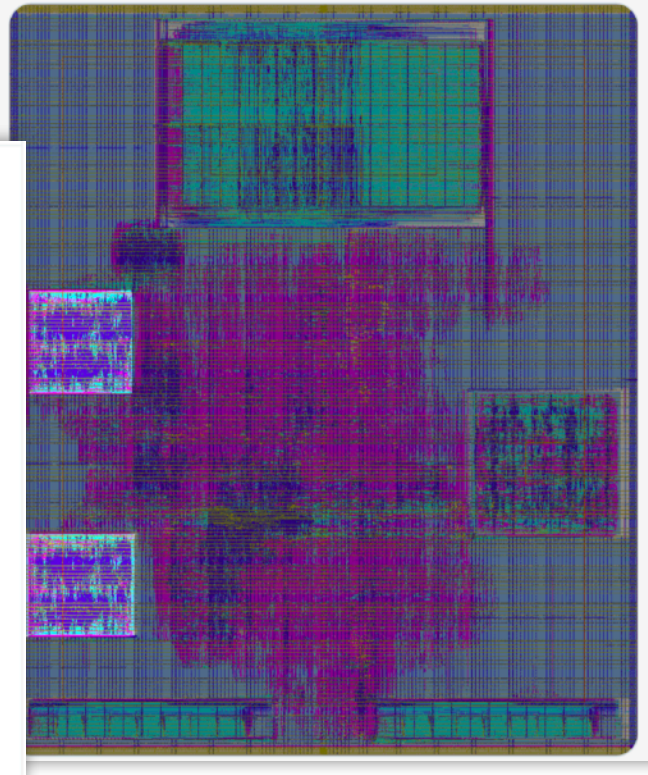
Watch the whole Caravel News below :-)
ef.link/iV1jd



Anton Blanchard @antonblanchard · Oct 12, 2022

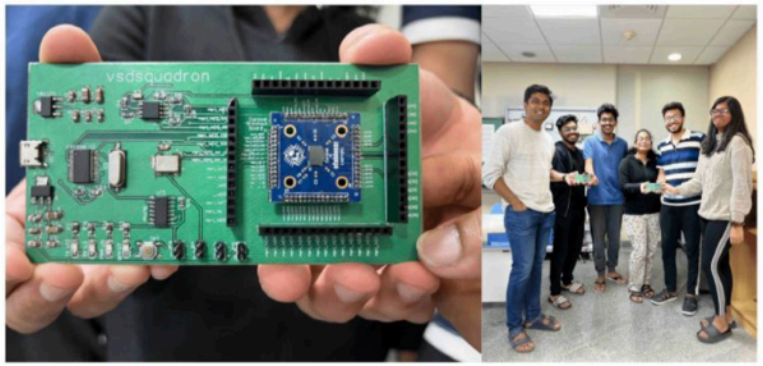
This came out of a need for a multiplier for the @OpenPOWERorg #Microwatt 64 bit processor for the @Google/@efabless/ @SkyWaterFoundry MPW shuttles.

#Microwatt has 2 64bit 2 cycle multiply-adders (one for fixed point and one for floating point).



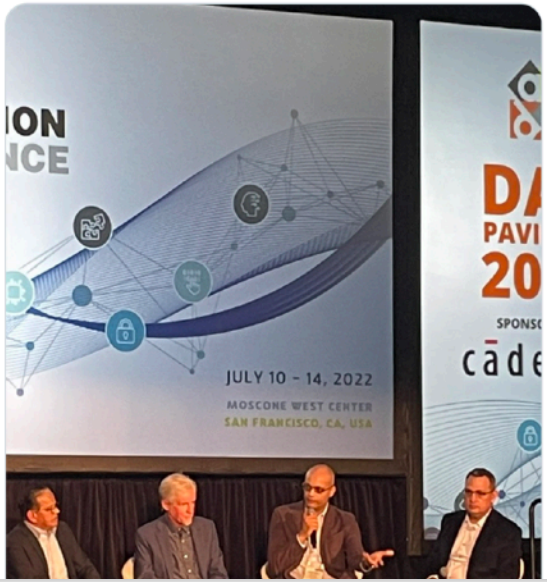
efabless.com @efabless · Jan 30

Curious about vsdsquadron, an educational board especially for RISC-V and semiconductor learning and training? Read blog by Kunal Ghosh.
bit.ly/3YaVrnR



GroupGets @groupgetscom · Jul 11, 2022

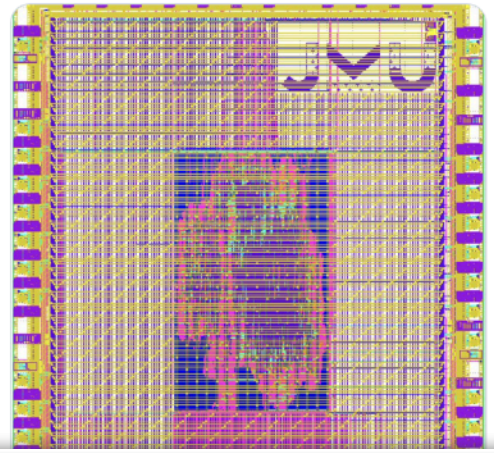
"Cloud is not for computing. It allows you to protect IP. It allows you to collaborate, and to experiment for more leads in the future." - Mohammad w/ @efabless on the Democritization of #Chip Design #59DAC



Matthew Venn @matthewvenn · Jan 26

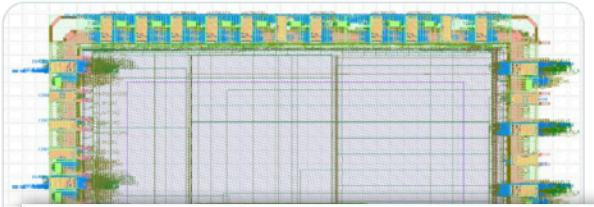
#OpenSourceASIChighlight @jkulinz implemented a stereo delta-sigma audio DAC. The digital DS-modulator features a single-bit output, and thus two digital GPIO (per channel) as outputs.

The design was designed for #Skywater130 and submitted to @Efabless MPW5.



James E. Stine, Jr. @JamesStineJr · Dec 19, 2020

Thanks to the hard work of my Ph.D. students Alex Underwood and Teo Ene, we were able to get a gds into the SkyWater/Google/**eFabless** run of our RISC-V single-cycle architecture thanks to @Google @efabless and @SkyWaterFoundry



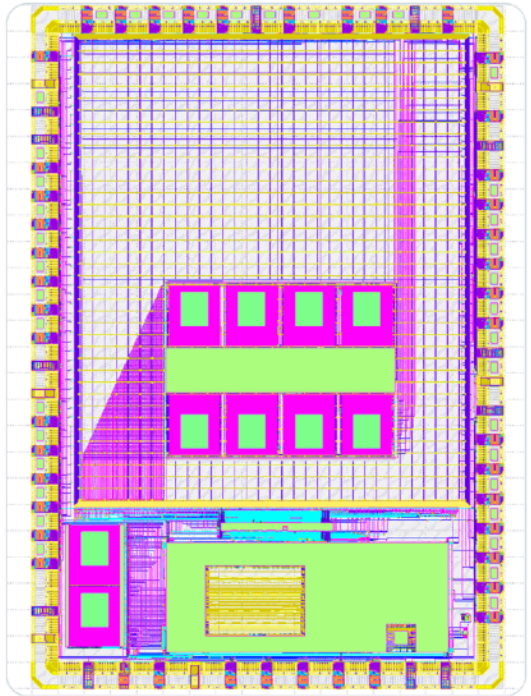
Michael Welling @m_w@chaos.... @QwertyEmb... · Nov 30, 2020

PyFive is about to take off on the @efabless @Google @SkyWaterFoundry shuttle.

Many thanks to @tnt for doing all of the work.

We waited on @UCSC_OpenRAM support for a bit too long but pivoted to bolting the peripherals carrier core this month.

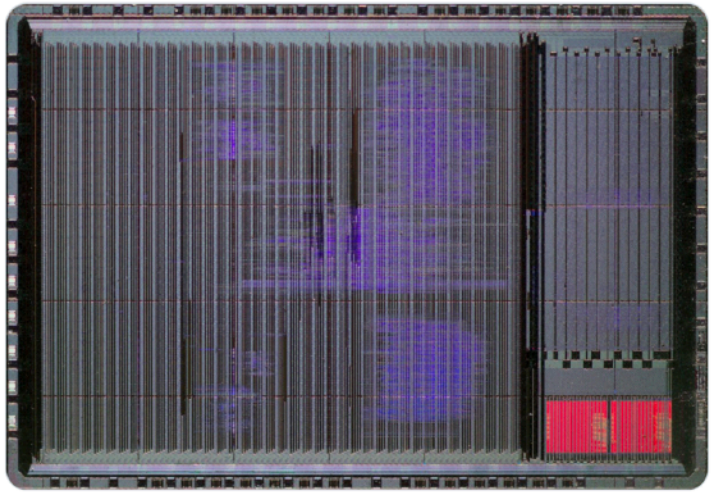
It has USB, audio, and video!



9 23 87

Anton Blanchard @antonblanchard · Mar 3, 2022

Thanks to @efabless, @Google and @SkyWaterFoundry for the chance to tape out #Microwatt, a 64 bit @OpenPOWERorg CPU, on #sky130_mpw1. Thanks also to the @OpenROAD_EDA and Openlane projects for the tools to make this possible. Open Hardware built with Open Source tools.



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IEEE SSC Society @SSCSociety · Jul 14, 2021

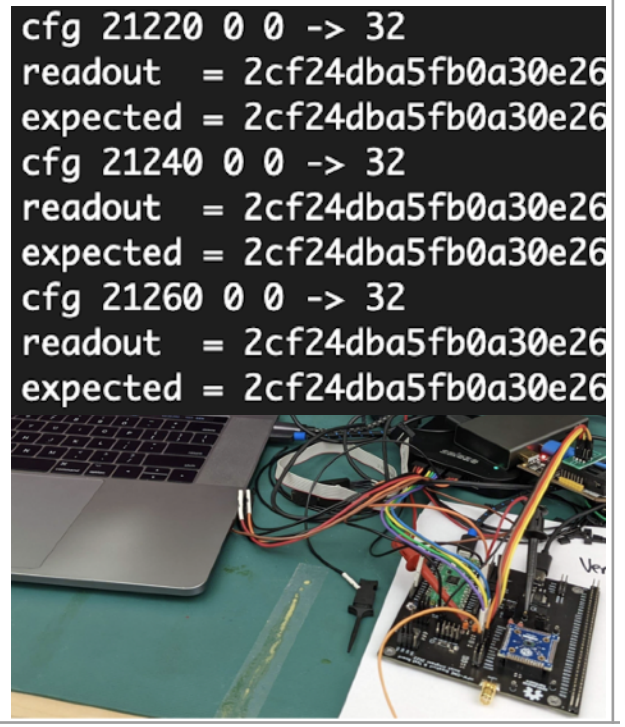
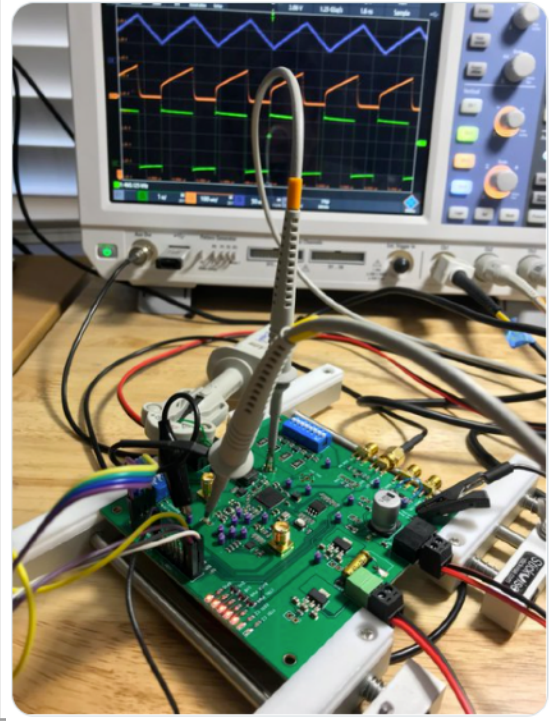
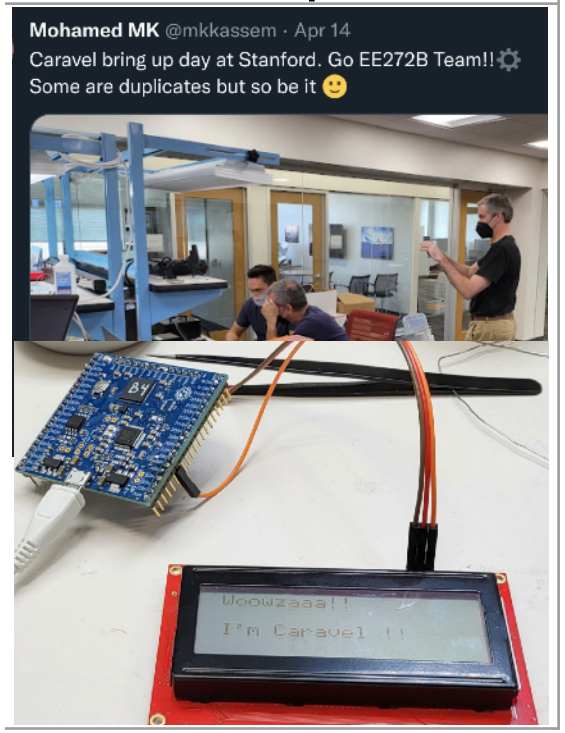
Call for Submissions for @SSCSociety Open-Source integrated circuit design contest. The final designs resulting from this contest will be submitted for 130 nm CMOS chip fabrication via **Efabless'** chipIgnite program. Deadline 7/30. More info: bit.ly/3yxY7PT.

IoT Guy @usmansarwar79 · Jan 29

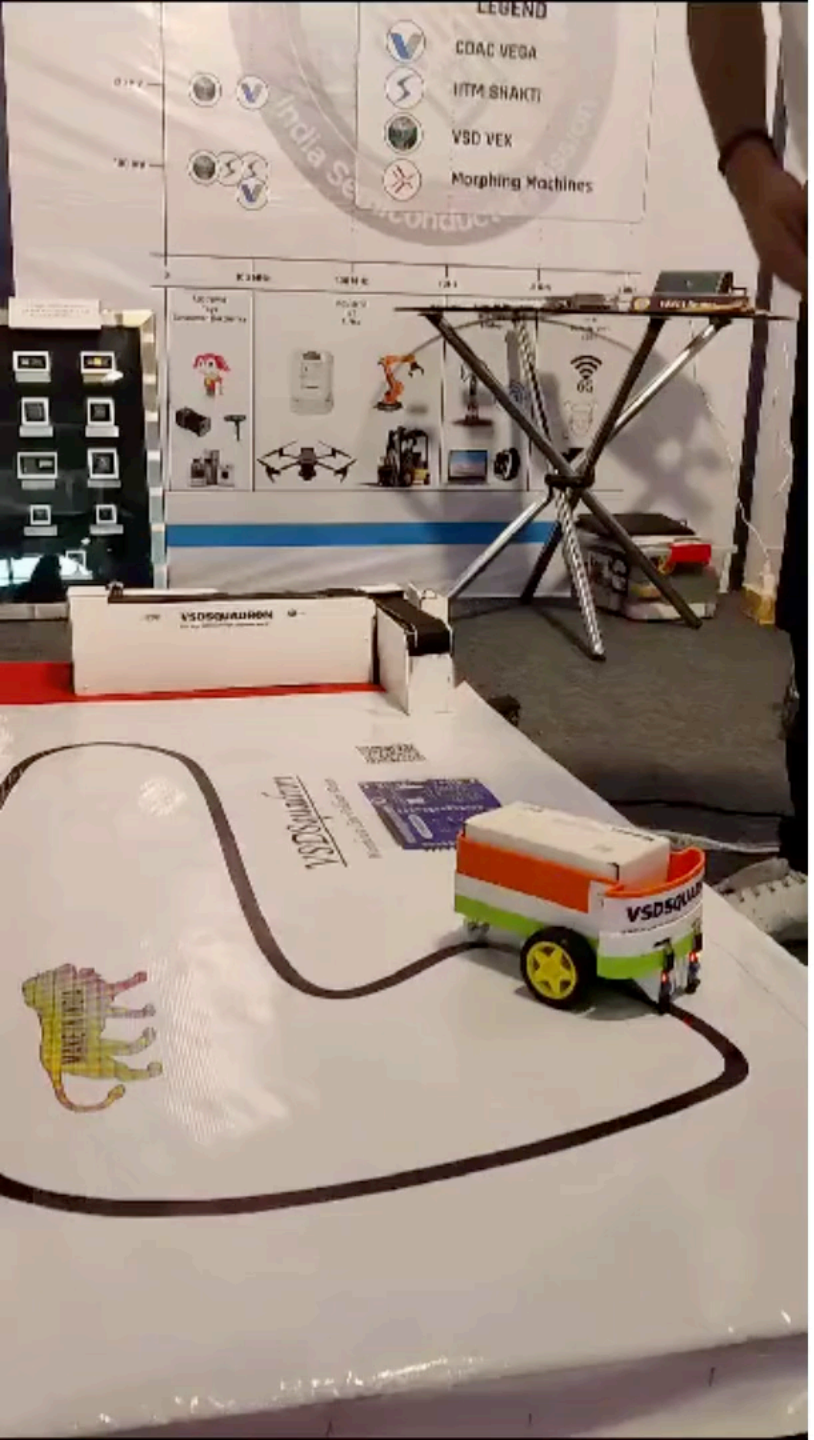
Would this make challenging business in future for conventional silicon manufacturer?
#iamintel #silicon #technologies

skywatertechnology.com
Google Partners with SkyWater and Efabless to Enable Open Sourc...
First open source foundry PDK enables full manufacturing chain for open hardware; Google-sponsored MPW shuttle program now ...

Returned **Silicon** —> library of “IP blocks”

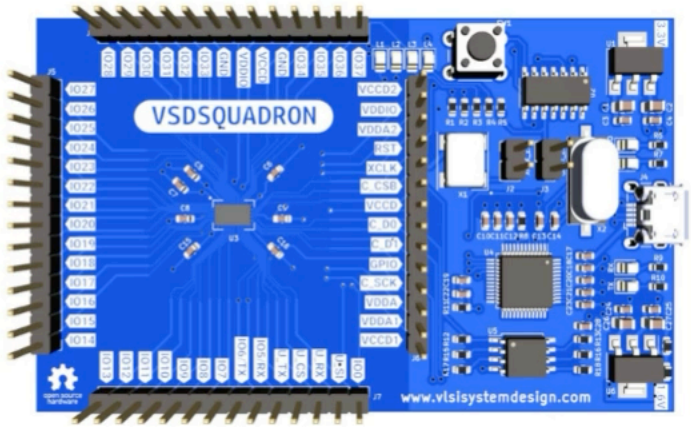
Person	Matt Venn	Anish Singhani	Weston Braun	Stanford EE272B
Shuttle	MPW-1	MPW-1	CIG-1	CIG-1
Project	Multiple	SHA256 & AES	PMIC	Multiple
	 			

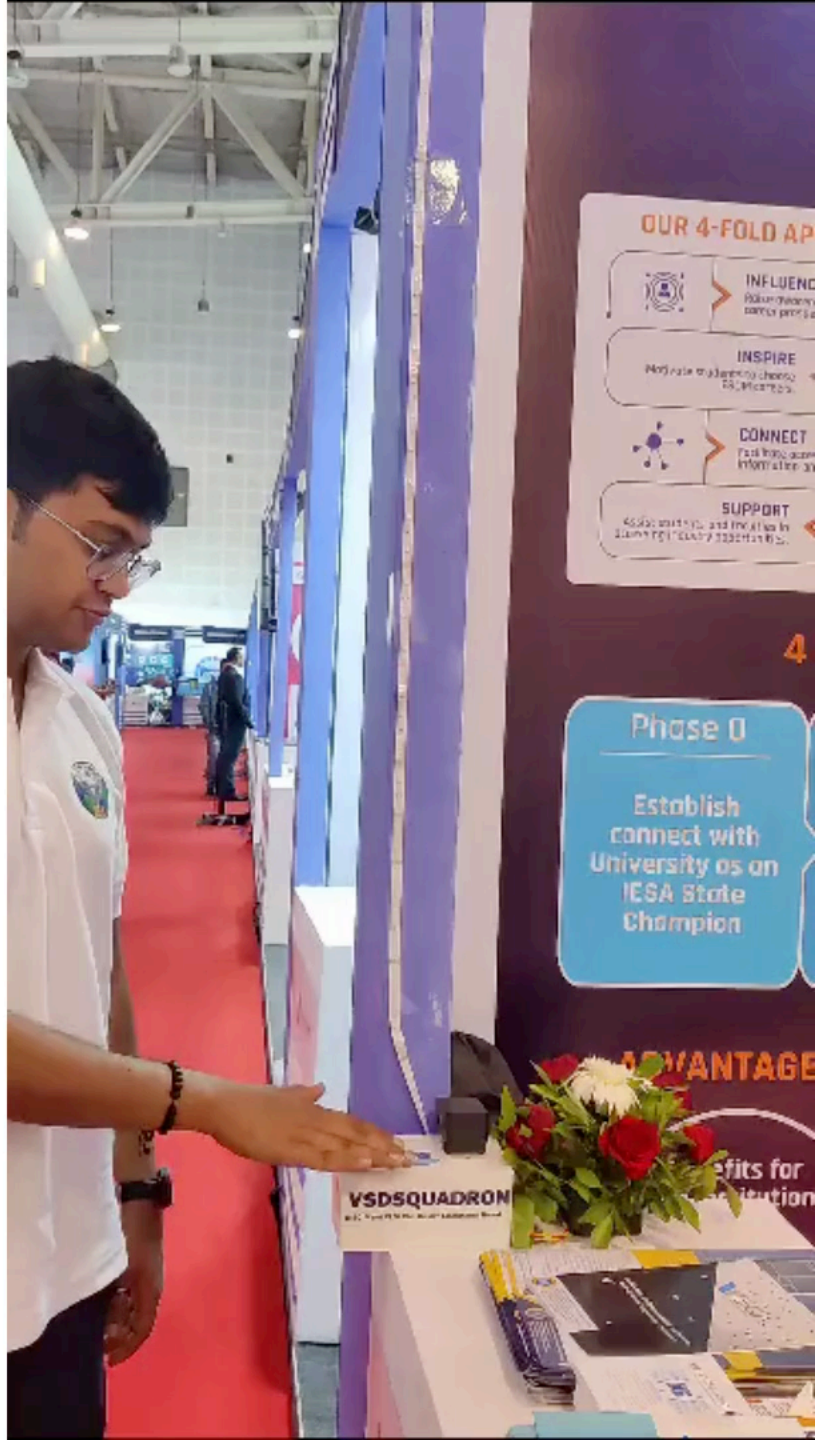
efabless.com



VSDSQUADRON

RISC-V and VLSI Chip Design Educational Board





Open Source Designs - Explosive Growth

April 2021 to Date

Fastest Ever *Design*

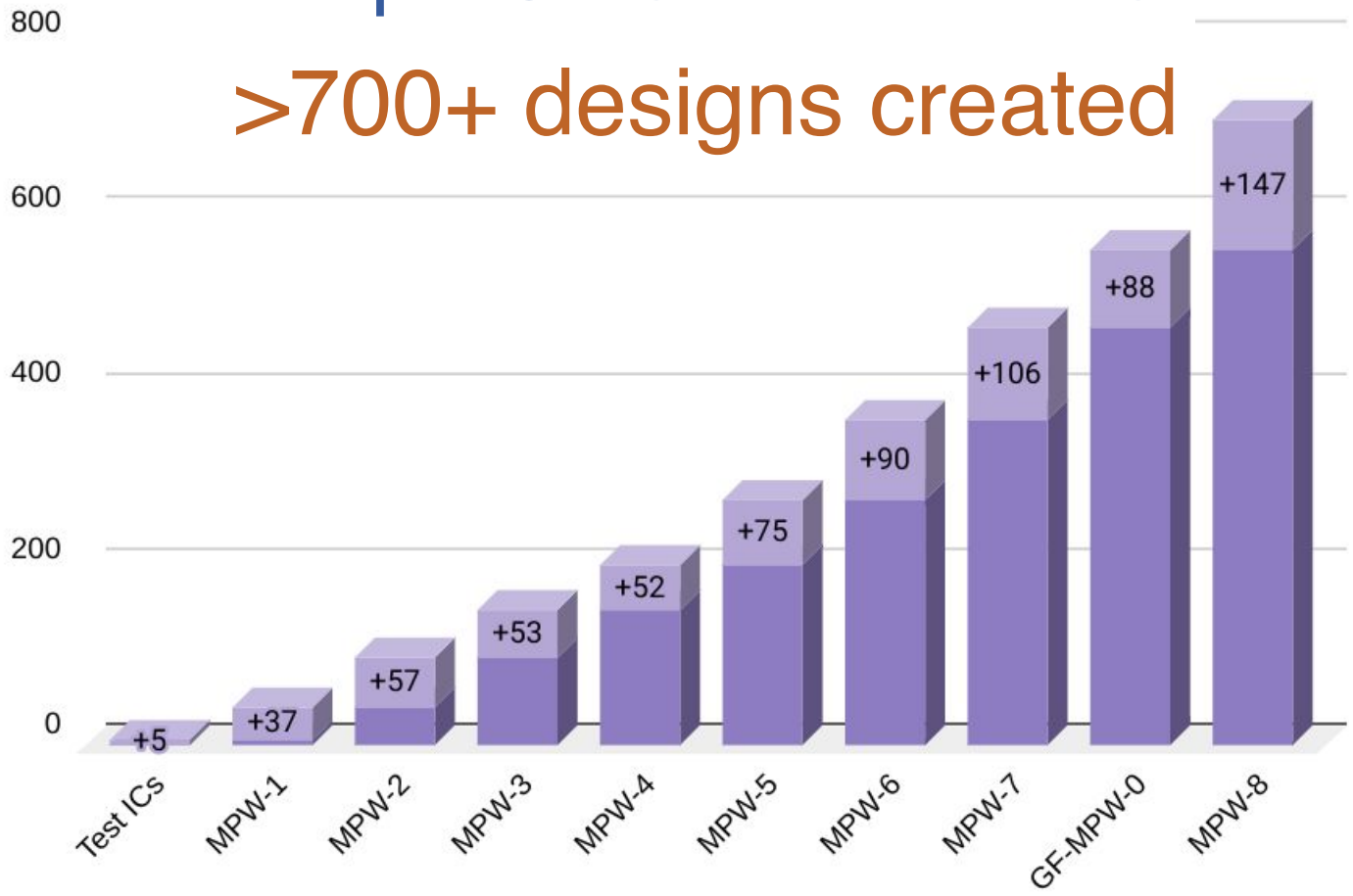
Creation Rate

Sponsored By:

Google

450 Tape-Outs In < 2 Years!

>700+ designs created



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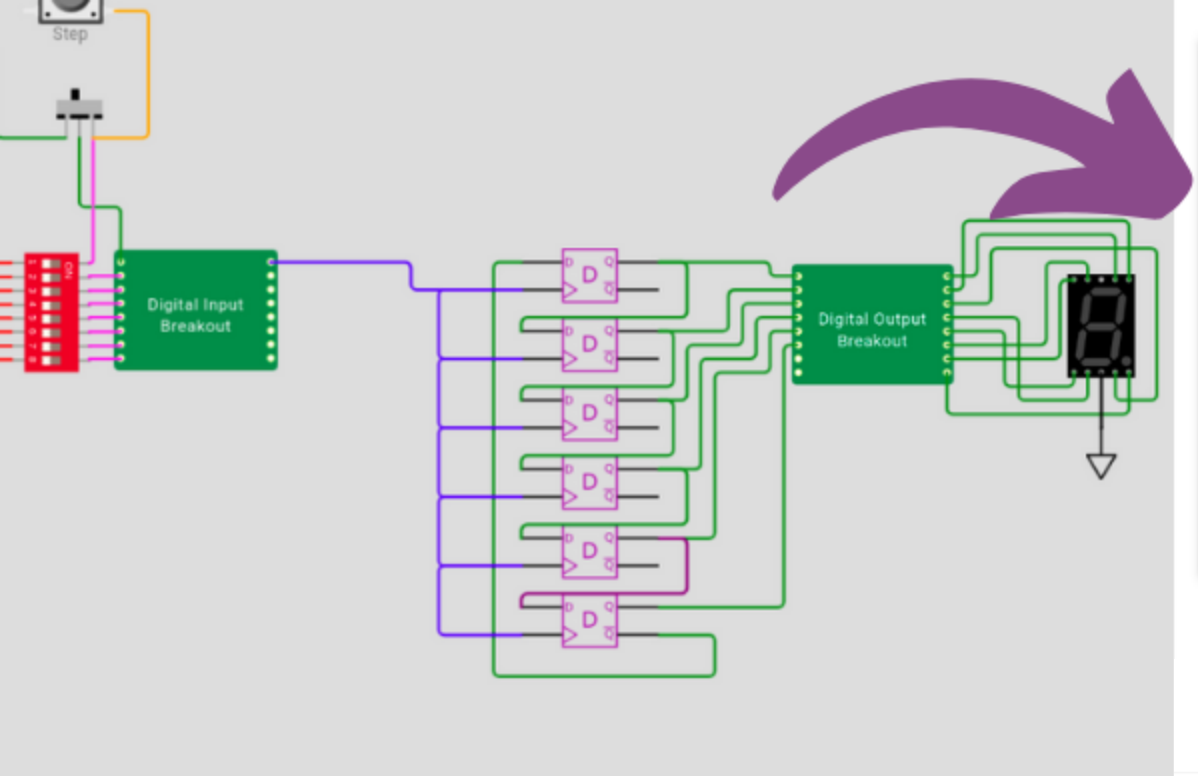
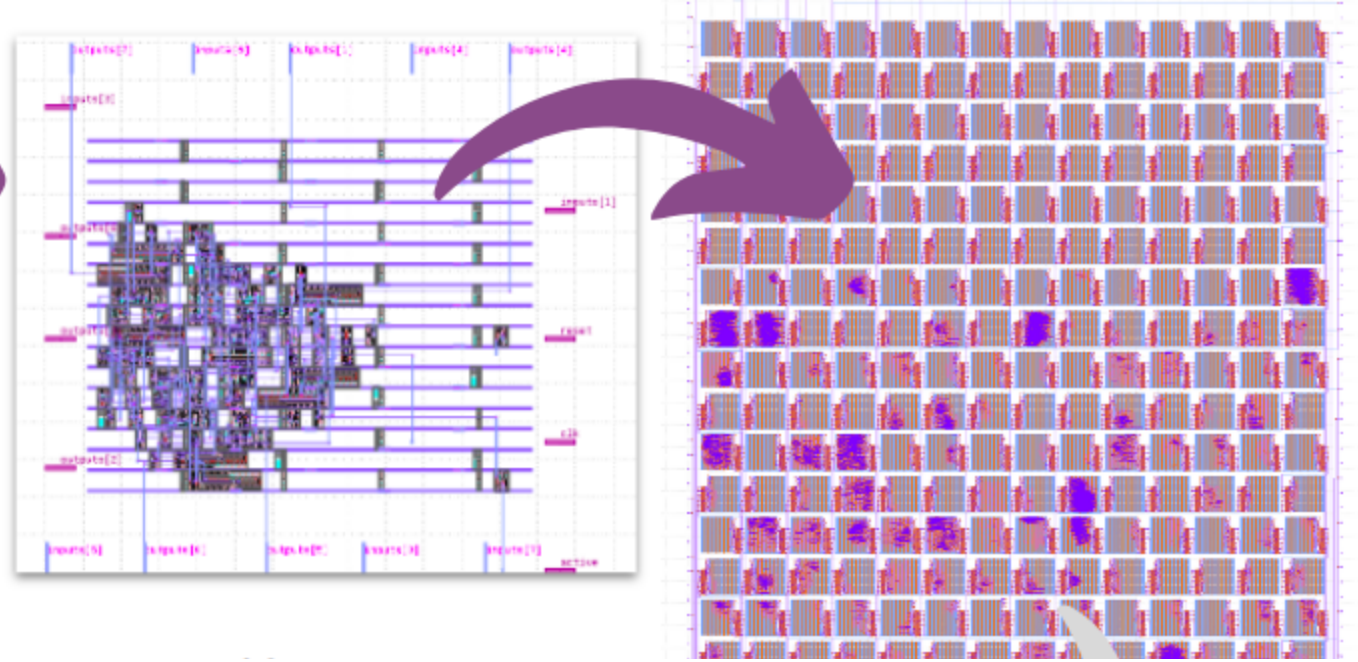
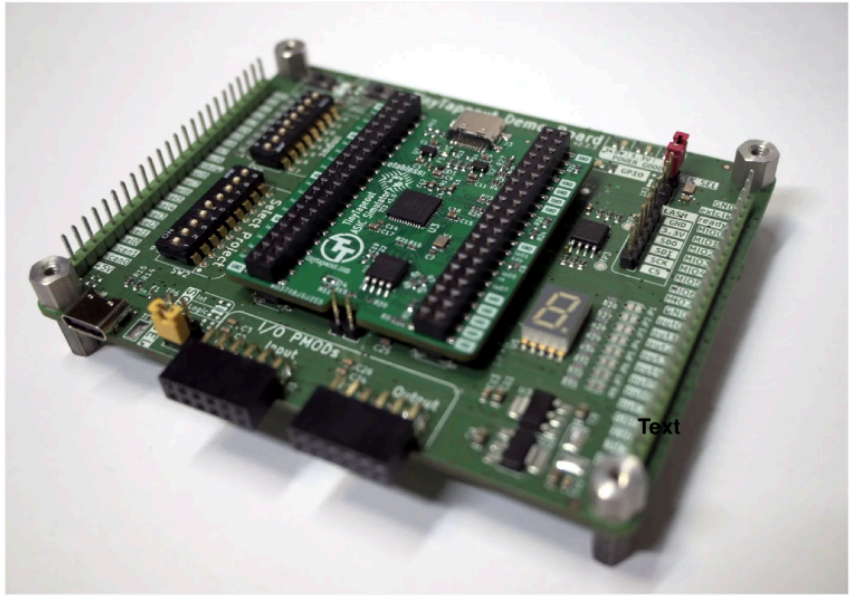




efabless

$300 ASIC

- Free access to design tools
- One (1) tile providing 160x100um up to 1000 standard cells
- Fabrication & packaging of your design in TinyTapeout chip
- One (1) demo board an ASIC carrier board
- A datasheet for all projects on the ASIC (100 projects)



EFABLESS

Tiny Tapeout

$300.00 USD

Quantity

1

Add to cart

Buy with Pay

More payment options

Purchase a Tiny Tapeout token today and embark on your journey of electronic innovation.

Community Developed Designs

Selected Open Source IP Blocks
A pseudo random number generator for critical real-time processors.
A General Purpose Bandgap generating constant voltage at output, independent of Temp and Supply variations.
Convolutional Neural Network Accelerator on a wishbone slave for Raven Core in Caravel SoC.
Maverick 603 Radio
Chaos automaton
Arduino pin compatible Single RISCV 32 Bit core Project
HSV to RGB color conversion accelerator
CMOS Bandgap
USB for RISC-V microcontroller
Analog Spiking Circuit and 10-bit DAC
Auditory perception acoustic front end
GPS Baseband
1V8 LDO
NAND Flash

Select Open Source SoCs
Sleep Apnea Detection System
Electro Mechanical Water Quality Monitoring
Influenza detector
Image Detection at Edge of Neural Networks
Satellite Radio
Epileptic Seizure Detection
LED Lighting for Bangladesh Solar Home System
Nanopore DNA Sequencing
Smart Garden
Industrial Motor Controller
Reconfigurable Flight Controller SoC for UAVs
TinyML Image Detection at Edge with DNN
Donkey Kong Bongo PS2 Keyboard

Select Industry Customer Applications

Customer Type	Application
Product	Quantum computing
Product	Data center encryption
Product	Automation
Chip	Proof of concept
Product	Air quality monitoring
Research	Memory
Product	Aerospace
Product	Blockchain
Chip	Security
Product	Data Encryption
Chip	Motion Sensor
Product	Datacenter PoC

Customer Type	Application
Product	Sensor
Product	Space
Chip	IoT SoC
Product	Proof of concept
Product	Medical Device
Product	Proof of concept
Product	Proof of concept
Chip	Active diode electronics
Product	Imaging sensor
Product	Secure SoC
Product	Multi-Language Keyboard
Product	Cryptocurrency mining
Product	Medical device
Product / chip	eFPGA module
Chip	Memory

10,000 community members

1200 designs

600 chips

3 years!

Empowering Collaborative Chip Design: Leveraging

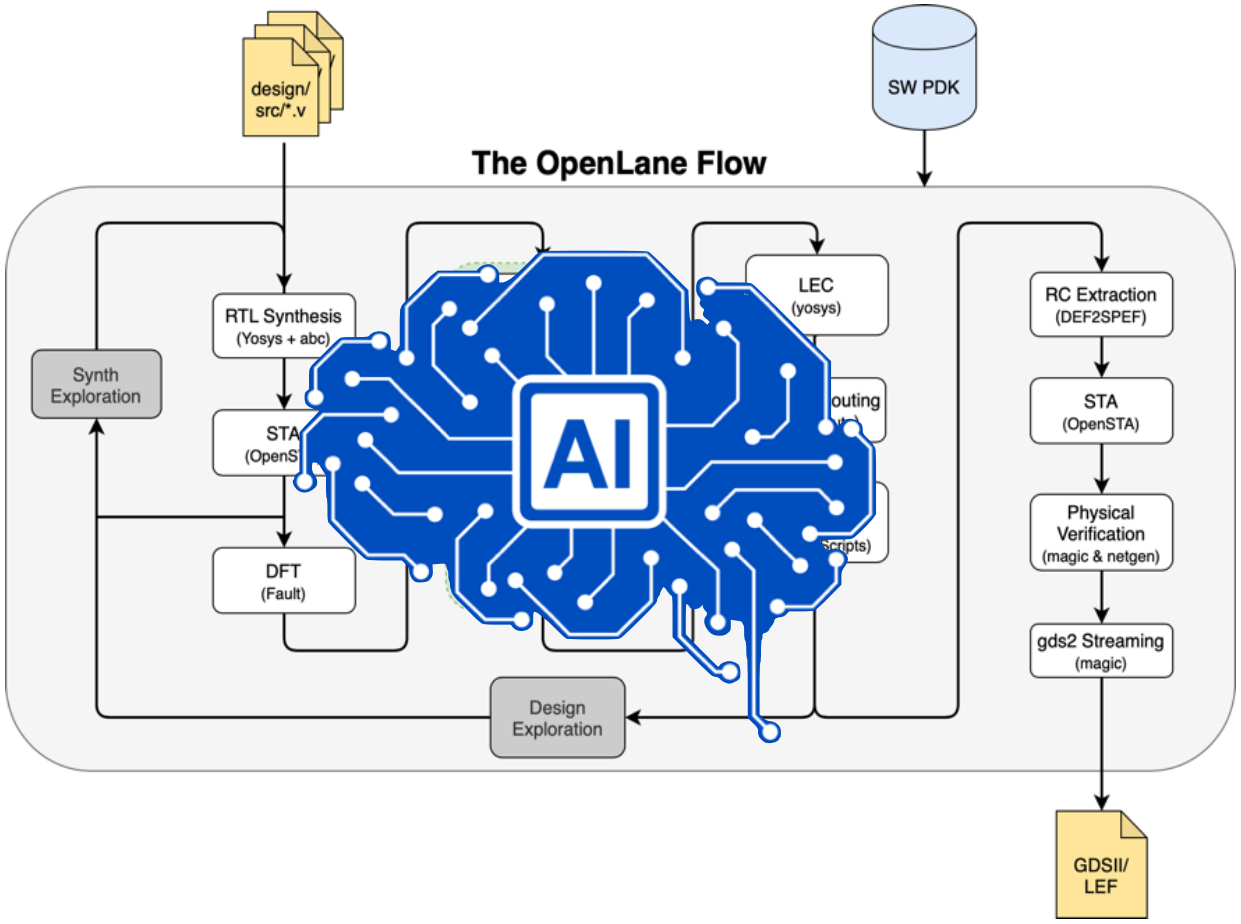
Generative AI for Custom Accelerators and Edge

AI Innovation

OpenLane DIGITAL COMPILER-LIKE RTL2GDS

Automate code-to-chip like a ***GNU software compiler - with trade-offs in area and performance.***

It opens the door for software developers to generate hardware
That's at least a 100x more potential designers!



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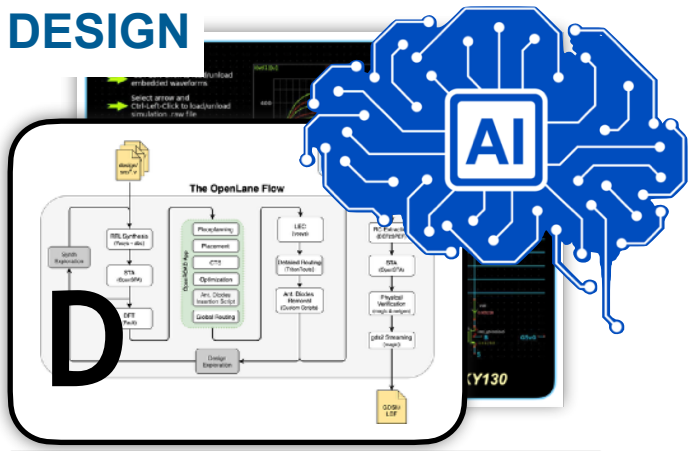
Complete & Path from Design to Test

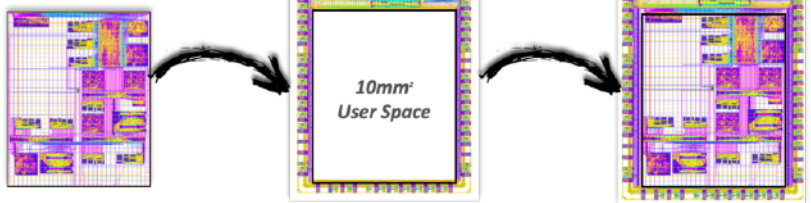
chipIgnite
Rapid IC Creation

1 DESIGN



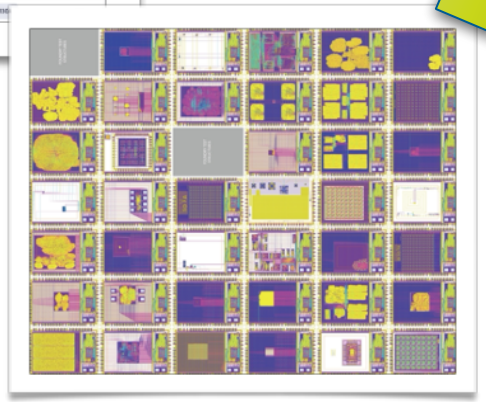
OS or Proprietary EDA Digital & Analog

2 INTEGRATE



3 SUBMIT

4 FABRICATE



5 TEST

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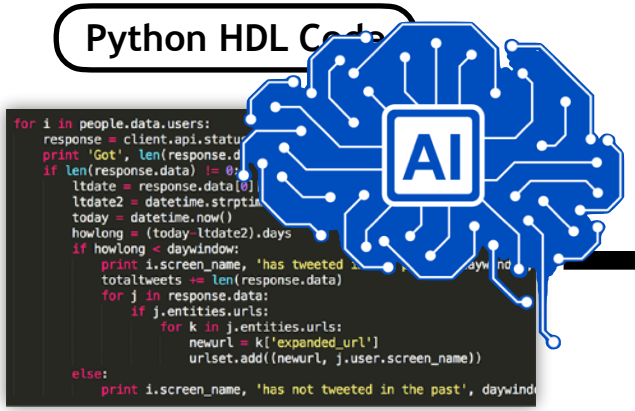
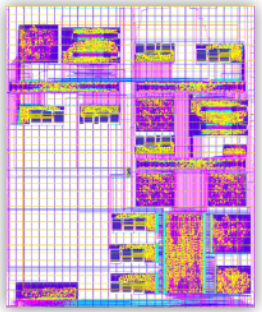
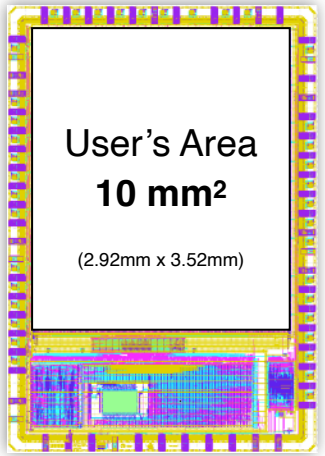
Design —> Code - Python <— LLM

Python HDL Code

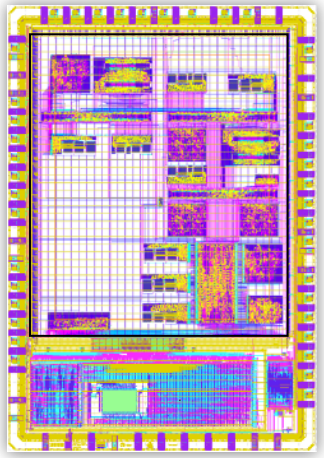




My Design



CARAVEL



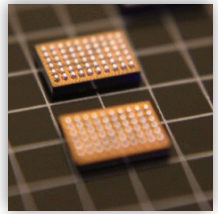
CARAVEL + My Design

MANUFACTURING

Software (FOSS)

Firmware

Plug and Play Dev Board



Parts

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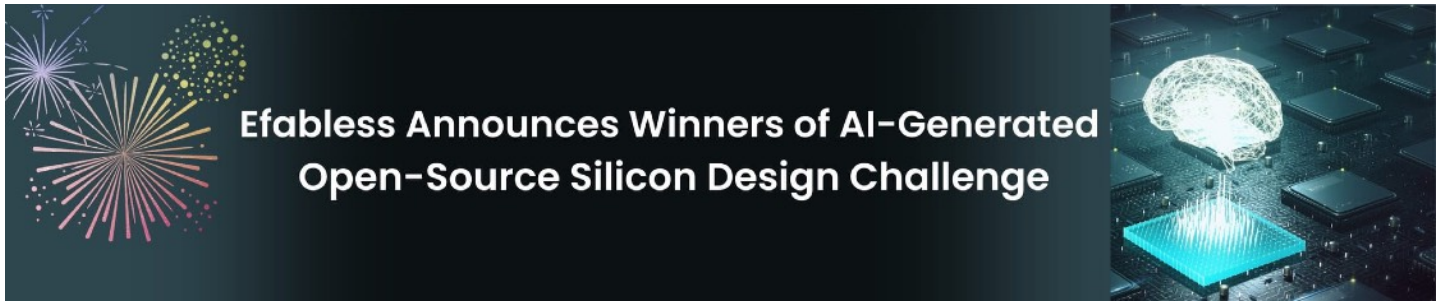
Challenge:

Lack of High quality

Open Source Data Set

Open Source Silicon with **GenAI**



~750 members

Many submissions were from teams

Only one had experience with ASIC Design

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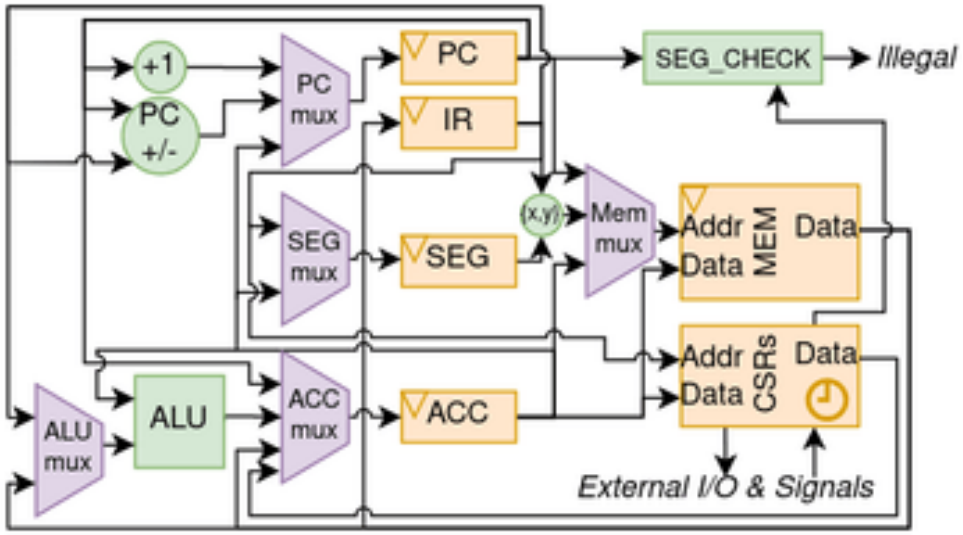
Design with **GenAI**

Open Source Silicon Design #1



1st Place: QTCore-C1

Hammond Pearce

The design is a co-processor that can be used for many applications, such as predictable-time I/O state machines for PIO functions as seen on some microcontrollers developed using the Chip-Chat methodology that the NYU team has published.

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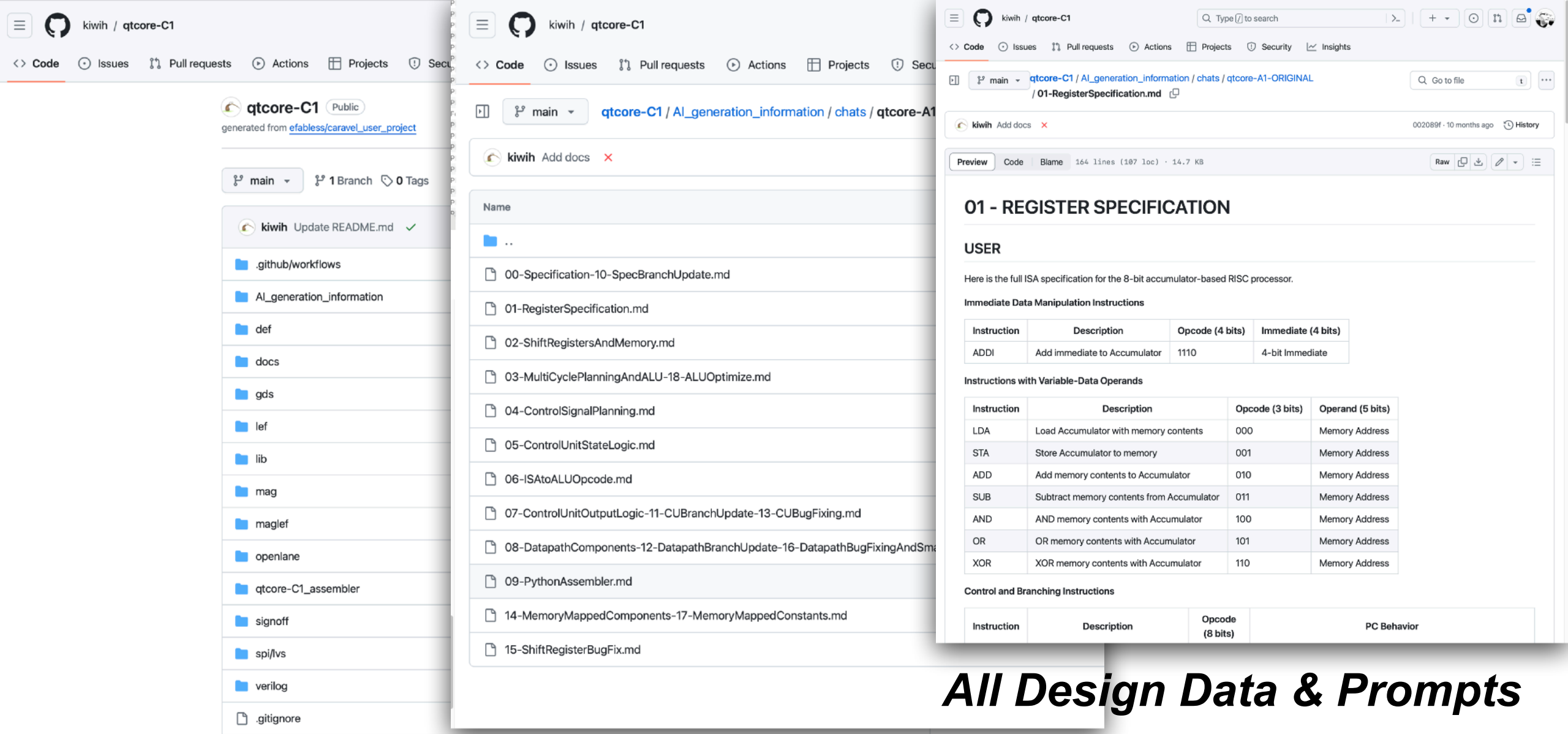

All Design Data & Prompts are Open Source

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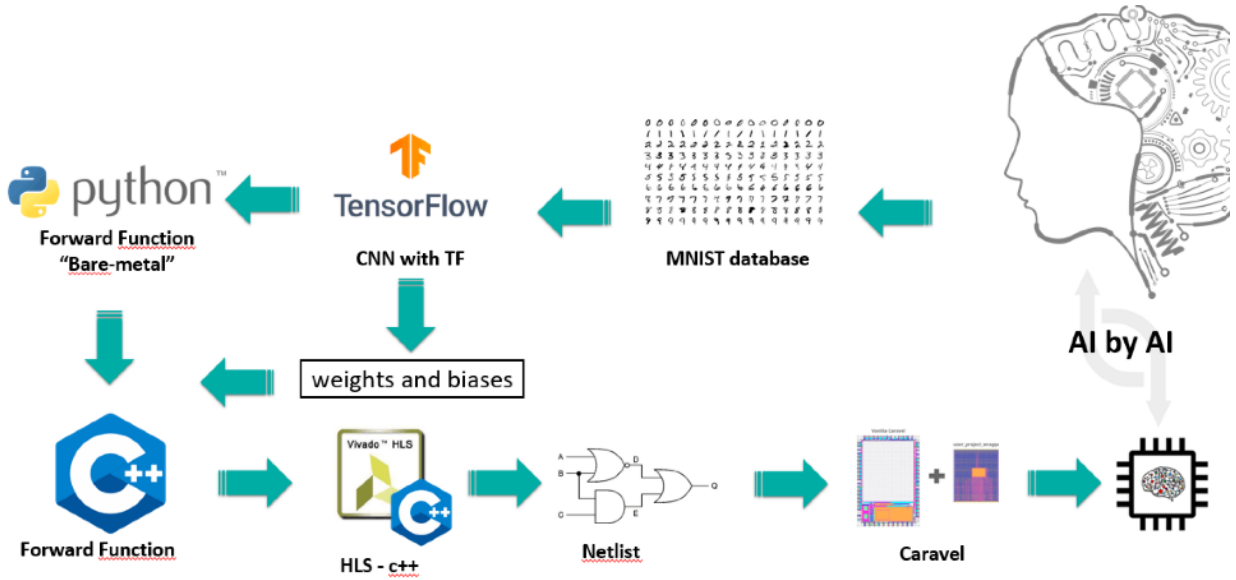
Design with **GenAI**

Open Source Silicon Design #2



1st Place: AI by AI

Emilio Isaac Baungarten Leon

The design is a dedicated hardware Integrated Circuit (IC) for a Convolutional Neural Network (CNN) that classifies the MNIST dataset written with the help of ChatGPT and documents the entire design process from the Python environment of TensorFlow to Verilog.

This approach demonstrates the incredible possibilities of AI-driven design.

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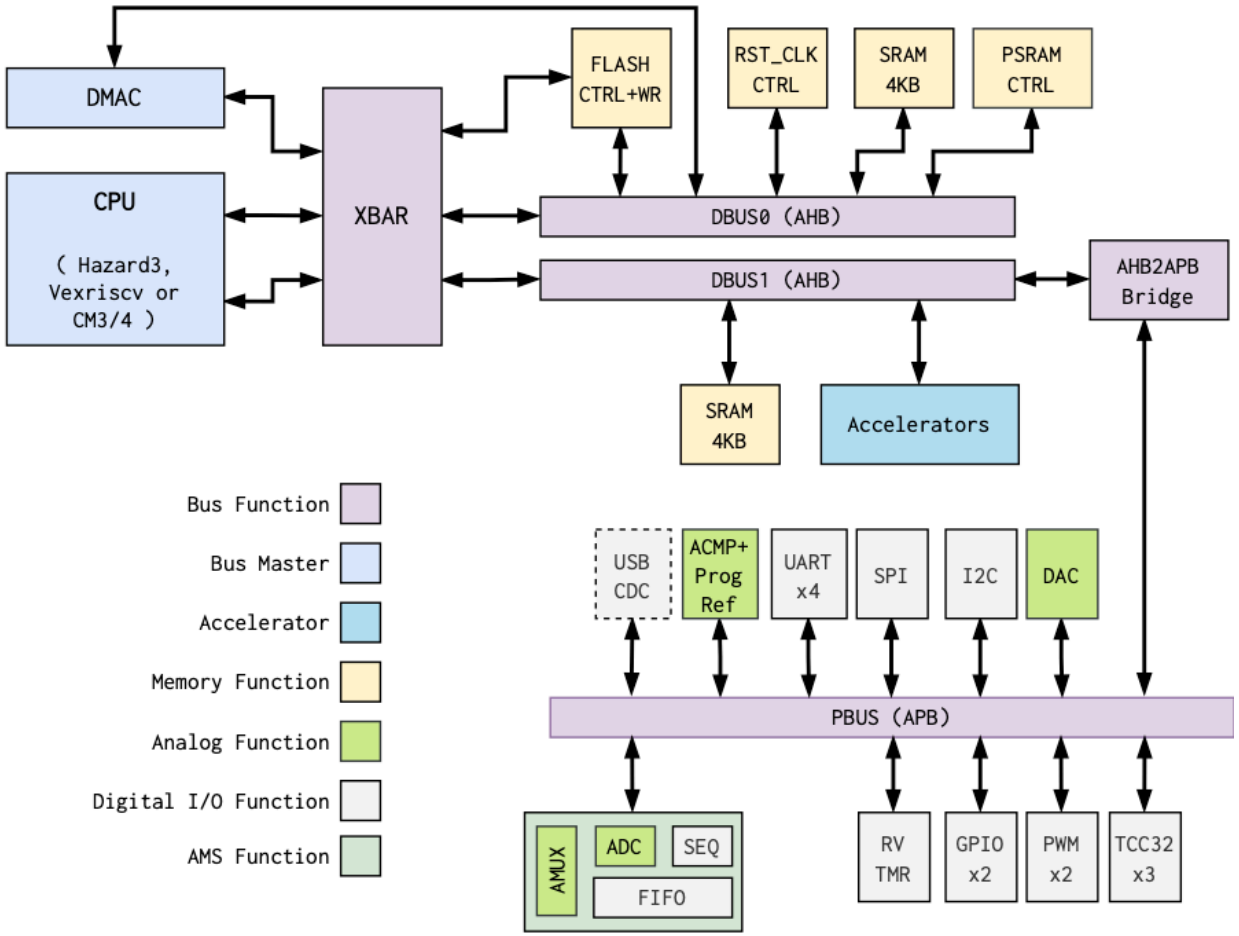
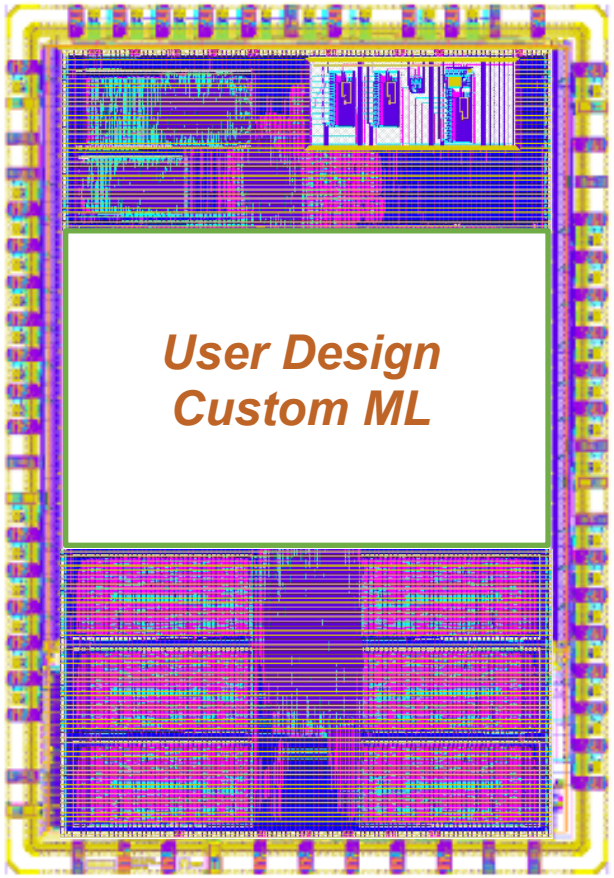
Don’t Start from scratch

Cheetah Open Source SoC for ML

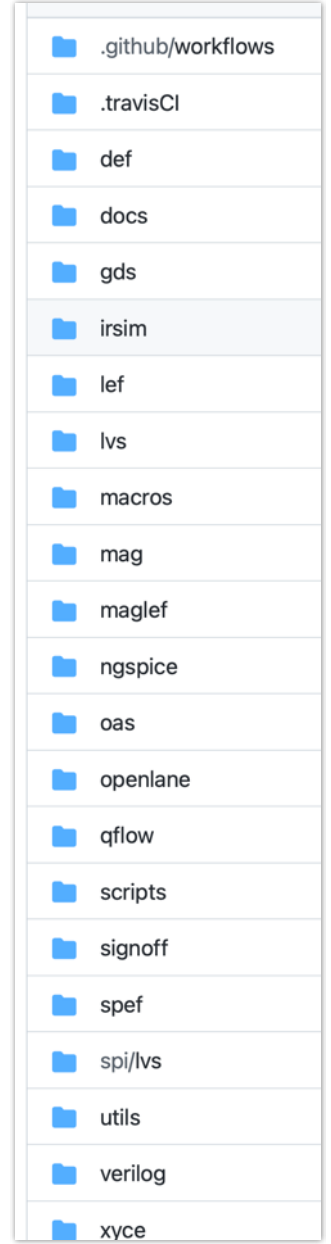


Low Power Advanced ML



Cheetah V3

Uniform Open Source File Structure to ease reuse & modifications



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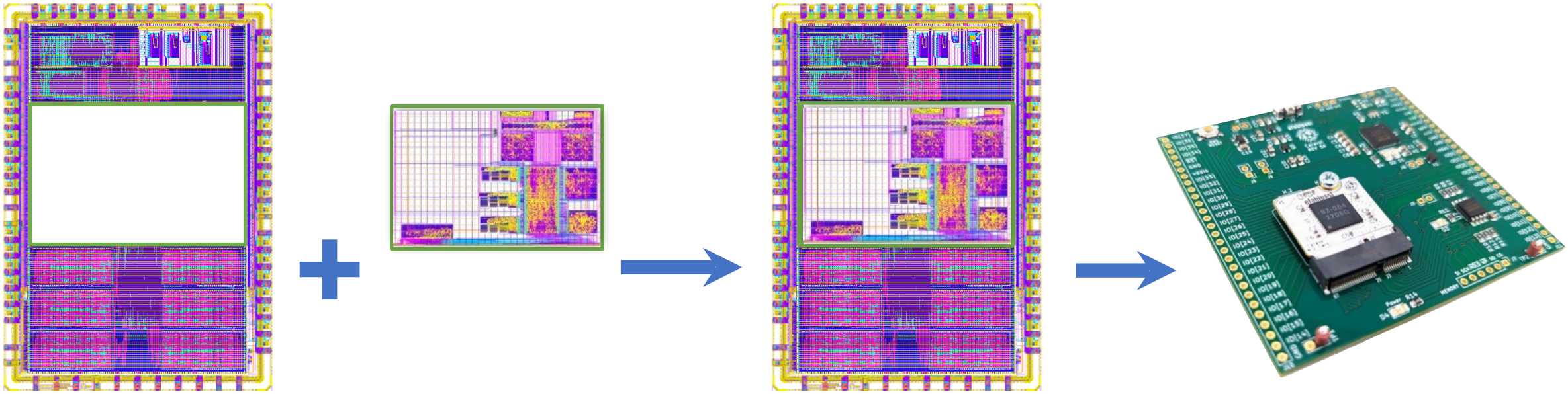
Cheetah Open Source SoC for ML

Reduce the knowledge ***Reduce the time*** ***Reduce the cost***



CHEETAH SoC

Your ML HW

CHEETAH + Your ML HW

Plug & Play Dev Board

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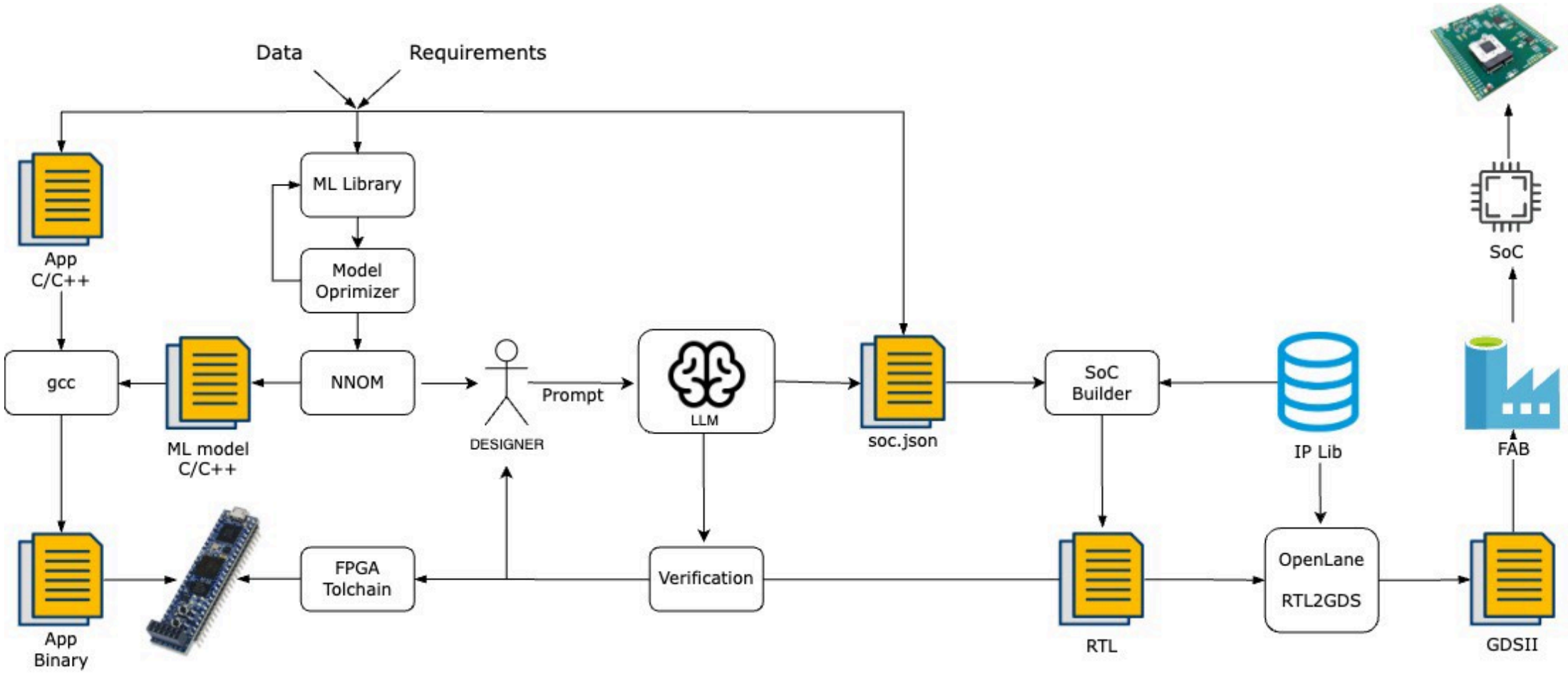
Design with **GenAI**

TinyML Inference

HW Accelerator Workflow



LLM with human driven prompts

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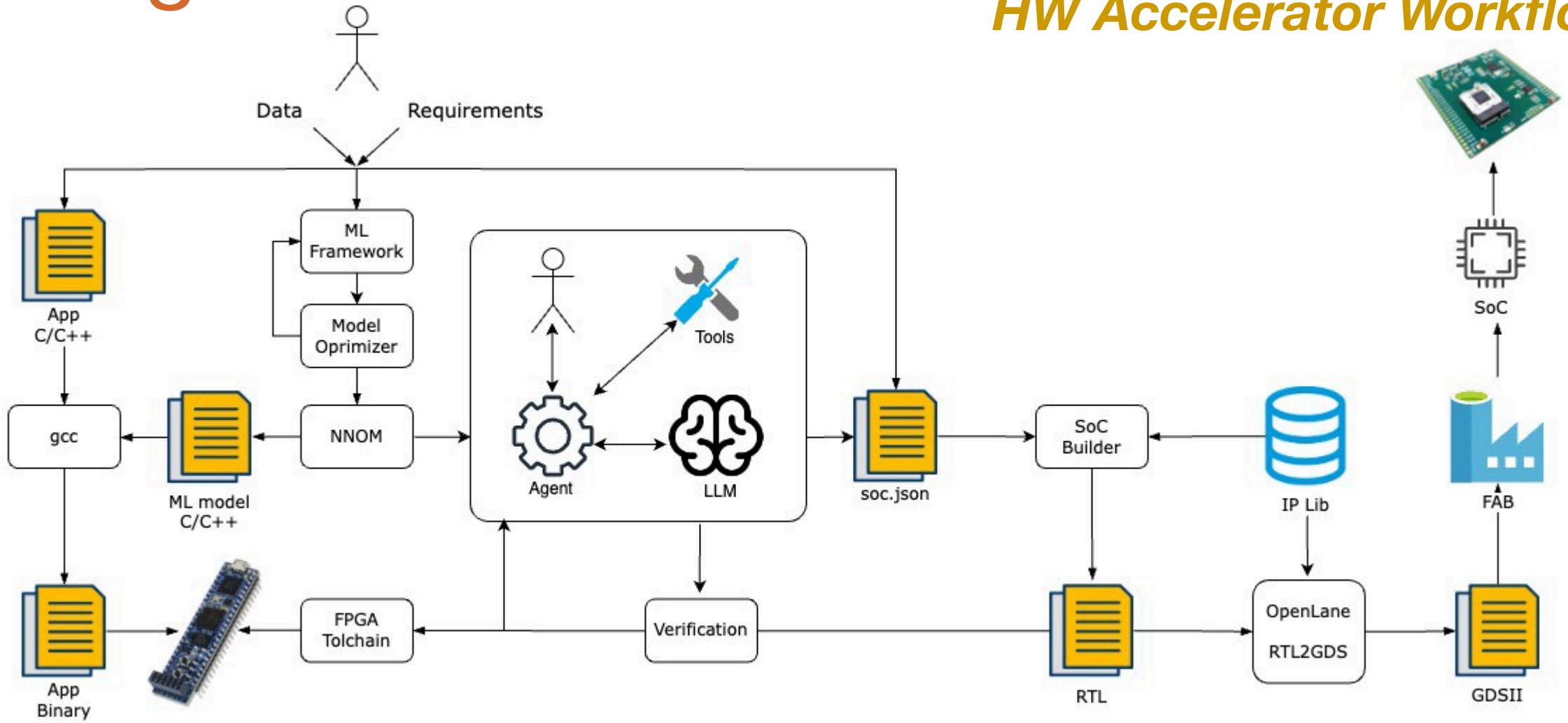
Design with **GenAI**

TinyML Inference

HW Accelerator Workflow



LLM + Agent + Human feedback

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Call to Action

Join the #generative-ai channel on https://oss.sc

Take on other challenge

You can get one done in hours

Contribute to the public dataset

Dataset generation?

Sponsor Open Source Design to Silicon?

GET TO SILICON

https://efabless.com