Empowering Collaborative Chip Design: Leveraging Generative AI for Custom Accelerators and Edge AI Innovation

Mohamed Kassem, Mohamed Shalan
mkk@efabless.com, mshalan@efabless.com
THE WORLD NEEDS CUSTOM CHIPS

CONSUMER
- Smart Home
- Entertainment
- Smart Recreation

INDUSTRIAL
- Smart Meters
- Agriculture
- Automotive

MEDICAL
- Wearable Devices
- Implantable Devices
- Telehealth Services

RETAIL
- Inventory Control
- Product Tracking
- Focused Marketing

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THE NEW GAME IS CUSTOM PRODUCTS

Markets Served By Traditional Methodology

Long-tail Innovation is required on a massive scale to meet demand 10,000’s of Products

Traditional custom chip development cost

Right-sized compute & power
THE NEW GAME IS CUSTOM PRODUCTS

Long-tail Innovation is required on a massive scale to meet demand 10,000’s of Products

Markets Served By Traditional Methodology

- Ideation
- Extreme Solutions
- Niche Markets
- AI
- ML

Right-sized compute & power

custom chip development cost with chipIgnite
Long-tail Innovation is required on a massive scale to meet demand for thousands of products.

THE NEW GAME IS CUSTOM PRODUCTS

Right-sized compute, power & cost
SEMICONDUCTOR INDUSTRY TRENDS

It's screaming "slow down innovation"

As Transistor Size Goes To Zero

Development Cost Goes to Infinity

Number of Customers Goes to Zero

Number of Designers Goes to Zero

Source: Mike Noonan
Unfortunately

Significant

Barriers Are In

The Way!

Not Enough Chip Designers

Design Costs Too Much

And Take Too Long
Empowering **Collaborative Chip Design**:

Leveraging Generative AI for Custom Accelerators and Edge AI Innovation
To simplify the process of Chip creation and make it accessible

To provide
- the business process
- the guardrails for quality
- the connection to customers
- the guardrails for IP protection
- the starting point - reference designs, IP
- the access to chip design tools flows, PDK & IP
- the scaleable & affordable cost structure

At least these 6 things must exist to create a chip.
Caravel Open Source SoC Platform

https://github.com/efabless/caravel

User's Project
~10 mm²
(2.92mm x 3.52mm)

Uniform Open Source File Structure to ease reuse & modifications

VexRISCV OpenRAM
OpenROAD OpenLane
One Size Fits All

**LOW COMPLEXITY**

- IP Development
- Digital & low frequency analog
- Enabling larger designer base

**HIGH COMPLEXITY**

- IP Development
- Complete Custom ASIC
- Analog & Digital
- Expert designer base

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OPEN SOURCE DESIGN FLOWS

- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD

- Schematic Capture
- SPICE Simulation

OpenLane

- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification
Automate code-to-chip like a **GNU software compiler** - with trade-offs in area and performance.

It opens the door for software developers to generate hardware. That’s at least a 100x more potential designers!
Complete & Path from Design to Test

1. DESIGN
   OS or Proprietary EDA Digital & Analog

2. INTEGRATE
   YOUR DESIGN

3. SUBMIT
   SUBMIT

4. FABRICATE
   CARAVEL
   CARAVEL

5. TEST
   TEST
COMMUNITY COLLABORATION

- Design house or community professional to set the specs
- Collaborate with other community members to create the design
- Prototype the solutions
- Publish the design solution in the marketplace

Community created IP, ICs and other HW products shared, licensed and forked
Clive (Max) Maxfield @MaxMaxfield · Jan 5
Developing the World’s First Commercially Available RF Device with an Open-Source Chip eejournal.com/article/develop... It’s great to see a small company use open-source tools and work with Efabless/SkyWater to develop a custom integrated circuit. @eetimes @MakerIO @hackaday @DesignNews

efabless.com @efabless · Jan 29
Glad to note that Klas Nordmark received his silicon :-) Klas an ASIC-adapted version of the award-winning bit-serial RF processor SERV. bit.ly/3XSEIdl
github.com/klasnordmark/c...
#icdesign #asics #ASIC

IWIRED Lab @ValpoWIREDlab · Apr 28, 2022
Our team’s SOURCE poster about their work coming up to speed with the @OpenROAD_EDA and @efabless OpenMPW open source VLSI toolchain. The groundwork for switching the full chip design course to these tools.

Michael Welling @m.w.chea... @QwertyEmbe... · Dec 29, 2021
The mpw-1 versions of the PyFive caravel chips have arrived.

Here are some images courtesy of @tnt.
Thanks to @efabless, @SkyWaterFoundry, @Google and everyone that helped make this possible.

Hopefully we can get working silicon in the near future.

#sky130 mpw1
It's a TAPEOUT!!! I have been informed, that my ASIC is accepted by @Efabless (MPW-8). The CUBE-V RISC-V CPU uses WAVE-PIPELINING and dynamic-interleaved multi-threading. A 25-year-old dream comes true. Thanks @Google for sponsorship + all the many helpers on Slack @OpenROAD_EDA

Anton Blanchard @antonblanchard · Oct 12, 2022
This came out of a need for a multiplier for the @OpenPOWERorg #Microwatt 64 bit processor for the @Google / @efabless / SkyWaterFoundry MPW shuttles.

#Microwatt has 2 64bit 2 cycle multiply-adders (one for fixed point and one for floating point).

Mohamed MK @mkkasem · Jul 8, 2022
#caravel is famous ... Local News TV Star! @NYSTECC @NYCreates NYDesign @efabless #chipignite

Watch the whole Caravel News below :-) ef.link/WTjd

efabless.com @efabless · Jan 30
Curious about vsdqsquadron, an educational board especially for RISC-V and semiconductor learning and training? Read blog by Kunal Ghosh. bit.ly/3YwMrR

GroupGets @groupgetscom · Jul 11, 2022
"Cloud is not for computing. It allows you to protect IP. It allows you to collaborate, and to experiment for more leads in the future." - Mohammad w. @efabless on the Democratization of Chip Design #58DAC
The design was designed for #Skywater130 and submitted to @Efabless MPW5.

Thanks to the hard work of my Ph.D. students Alex Underwood and Teo Ene, we were able to get a gds into the SkyWater/Google/EFabless run of our RISC-V single-cycle architecture thanks to @Google @efabless and @SkyWaterFoundry.

Pyfive is about to take off on the @efabless @Google @SkyWaterFoundry shuttle.

Many thanks to @ntt for doing all of the work.

We waited on @UCSC_OpenSource support for a bit too long but pivoted to bolting the peripherals carrier core this month.

It has USB, audio, and video!
Returned **Silicon** —> library of “IP blocks”

<table>
<thead>
<tr>
<th>Person</th>
<th>Matt Venn</th>
<th>Anish Singhani</th>
<th>Weston Braun</th>
<th>Stanford EE272B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shuttle</td>
<td>MPW-1</td>
<td>MPW-1</td>
<td>CIG-1</td>
<td>CIG-1</td>
</tr>
<tr>
<td>Project</td>
<td>Multiple</td>
<td>SHA256 &amp; AES</td>
<td>PMIC</td>
<td>Multiple</td>
</tr>
</tbody>
</table>

```
cfg 21220 0 0 -> 32
readout = 2cf24dba5fb0a30e26
expected = 2cf24dba5fb0a30e26
cfg 21240 0 0 -> 32
readout = 2cf24dba5fb0a30e26
expected = 2cf24dba5fb0a30e26
cfg 21260 0 0 -> 32
readout = 2cf24dba5fb0a30e26
expected = 2cf24dba5fb0a30e26
```
VSDSQUADRON
RISC-V and VLSI Chip Design Educational Board
Open Source Designs - Explosive Growth

April 2021 to Date

Fastest Ever Design Creation Rate

Sponsored By: Google

450 Tape-Outs In < 2 Years!

>700+ designs created
$300 ASIC

- Free access to design tools
- One (1) tile providing 160x100um up to 1000 standard cells
- Fabrication & packaging of your design in TinyTapeout chip
- One (1) demo board an ASIC carrier board
- A datasheet for all projects on the ASIC (100 projects)
Selected Open Source IP Blocks

- A pseudo random number generator for critical real-time processors.
- A General Purpose Bandgap generating constant voltage at output, independent of Temp and Supply variations.
- Convolutional Neural Network Accelerator on a wishbone slave for Raven Core in Caravel SoC.
- Maverick 603 Radio
- Chaos automaton
- Arduino pin compatible Single RISCV 32 Bit core Project
- HSV to RGB color conversion accelerator
- CMOS Bandgap
- USB for RISC-V microcontroller
- Analog Spiking Circuit and 10-bit DAC
- Auditory perception acoustic front end
- GPS Baseband
- 1V LDO
- NAND Flash

Select Open Source SoCs

- Sleep Apnea Detection System
- Electro Mechanical Water Quality Monitoring
- Influenza detector
- Image Detection at Edge of Neural Networks
- Satellite Radio
- Epileptic Seizure Detection
- LED Lighting for Bangladesh Solar Home System
- Nanopore DNA Sequencing
- Smart Garden
- Industrial Motor Controller
- Reconfigurable Flight Controller SoC for UAVs
- TinyML Image Detection at Edge with DNN
- Donkey Kong Bongo PS2 Keyboard

Community Developed Designs
<table>
<thead>
<tr>
<th>Customer Type</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product</td>
<td>Quantum computing</td>
</tr>
<tr>
<td>Product</td>
<td>Data center encryption</td>
</tr>
<tr>
<td>Product</td>
<td>Automation</td>
</tr>
<tr>
<td>Chip</td>
<td>Proof of concept</td>
</tr>
<tr>
<td>Product</td>
<td>Air quality monitoring</td>
</tr>
<tr>
<td>Research</td>
<td>Memory</td>
</tr>
<tr>
<td>Product</td>
<td>Aerospace</td>
</tr>
<tr>
<td>Product</td>
<td>Blockchain</td>
</tr>
<tr>
<td>Chip</td>
<td>Security</td>
</tr>
<tr>
<td>Product</td>
<td>Data Encryption</td>
</tr>
<tr>
<td>Chip</td>
<td>Motion Sensor</td>
</tr>
<tr>
<td>Product</td>
<td>Datacenter PoC</td>
</tr>
</tbody>
</table>

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<th>Customer Type</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Product</td>
<td>Sensor</td>
</tr>
<tr>
<td>Product</td>
<td>Space</td>
</tr>
<tr>
<td>Chip</td>
<td>IoT SoC</td>
</tr>
<tr>
<td>Product</td>
<td>Proof of concept</td>
</tr>
<tr>
<td>Product</td>
<td>Medical Device</td>
</tr>
<tr>
<td>Product</td>
<td>Proof of concept</td>
</tr>
<tr>
<td>Product</td>
<td>Proof of concept</td>
</tr>
<tr>
<td>Chip</td>
<td>Active diode electronics</td>
</tr>
<tr>
<td>Product</td>
<td>Imaging sensor</td>
</tr>
<tr>
<td>Product</td>
<td>Secure SoC</td>
</tr>
<tr>
<td>Product</td>
<td>Multi-Language Keyboard</td>
</tr>
<tr>
<td>Product</td>
<td>Cryptocurrency mining</td>
</tr>
<tr>
<td>Product</td>
<td>Medical device</td>
</tr>
<tr>
<td>Product / chip</td>
<td>eFPGA module</td>
</tr>
<tr>
<td>Chip</td>
<td>Memory</td>
</tr>
</tbody>
</table>
10,000 community members
1200 designs
600 chips
3 years!
Empowering Collaborative Chip Design: Leveraging Generative AI for Custom Accelerators and Edge AI Innovation
Automate code-to-chip like a **GNU software compiler** - with trade-offs in area and performance.

It opens the door for software developers to generate hardware. That’s at least a **100x** more potential designers!
Complete & Path from Design to Test

1. DESIGN
   OS or Proprietary EDA Digital & Analog

2. INTEGRATE
   YOUR DESIGN

3. SUBMIT
   CARAVEL

4. FABRICATE
   CARAVEL

5. TEST
   chipIgnite
   Rapid IC Creation
Design -> Code - Python <-> LLM

Python HDL Code

My Design + CARAVEL

User's Area 10 mm²
(2.92mm x 3.52mm)

CARAVEL + My Design

MANUFACTURING

Software (FOSS)

Plug and Play Dev Board

Firmware

Parts
Challenge:

Lack of High quality Open Source Data Set
Open Source Silicon with GenAI

Efabless Announces Winners of AI-Generated Open-Source Silicon Design Challenge

The Winners of the 2nd AI Generated Design Contest Announced!

Winners Announced!
3rd AI Generated Silicon Design Challenge

~750 members
Many submissions were from teams
Only one had experience with ASIC Design
The design is a co-processor that can be used for many applications, such as predictable-time I/O state machines for PIO functions as seen on some microcontrollers developed using the Chip-Chat methodology that the NYU team has published.
01 - REGISTER SPECIFICATION

USER

Here is the full ISA specification for the 8-bit accumulator-based RISC processor.

Immediate Data Manipulation Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Opcode (4 bits)</th>
<th>Immediate (4 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>Add Immediate to Accumulator</td>
<td>1110</td>
<td>4-bit Immediate</td>
</tr>
</tbody>
</table>

Instructions with Variable-Data Operands

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Opcode (3 bits)</th>
<th>Operand (5 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDA</td>
<td>Load Accumulator with memory contents</td>
<td>000</td>
<td>Memory Address</td>
</tr>
<tr>
<td>STA</td>
<td>Store Accumulator to memory</td>
<td>001</td>
<td>Memory Address</td>
</tr>
<tr>
<td>ADD</td>
<td>Add memory contents to Accumulator</td>
<td>010</td>
<td>Memory Address</td>
</tr>
<tr>
<td>SUB</td>
<td>Subtract memory contents from Accumulator</td>
<td>011</td>
<td>Memory Address</td>
</tr>
<tr>
<td>AND</td>
<td>AND memory contents with Accumulator</td>
<td>100</td>
<td>Memory Address</td>
</tr>
<tr>
<td>OR</td>
<td>OR memory contents with Accumulator</td>
<td>101</td>
<td>Memory Address</td>
</tr>
<tr>
<td>XOR</td>
<td>XOR memory contents with Accumulator</td>
<td>110</td>
<td>Memory Address</td>
</tr>
</tbody>
</table>

Control and Branching Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Opcode (8 bits)</th>
<th>PC Behavior</th>
</tr>
</thead>
</table>

All Design Data & Prompts are Open Source
The design is a dedicated hardware Integrated Circuit (IC) for a Convolutional Neural Network (CNN) that classifies the MNIST dataset written with the help of ChatGPT and documents the entire design process from the Python environment of TensorFlow to Verilog.

This approach demonstrates the incredible possibilities of AI-driven design.
Don’t Start from scratch
Cheetah Open Source SoC for ML

Uniform Open Source File Structure to ease reuse & modifications

Low Power Advanced ML

Cheetah V3
Cheetah Open Source SoC for ML

Reduce the knowledge  Reduce the time  Reduce the cost

CHEETAH SoC  Your ML HW  CHEETAH + Your ML HW  Plug & Play Dev Board
Design with **GenAI**

TinyML Inference

HW Accelerator Workflow

LLM with human driven prompts
Design with **GenAI**

**TinyML Inference**

**HW Accelerator Workflow**

**LLM + Agent + Human feedback**
Call to Action

Join the #generative-ai channel on https://oss.sc

Take on other challenge
You can get one done in hours

Contribute to the public dataset

Create a Hardware Accelerator for Keyword Spotting with Generative AI

Awarding up to $30,000 of chipIgnite silicon
Dataset generation?

Sponsor Open Source Design to Silicon?
GET TO SILICON

https://efabless.com