Thank you, tinyML Strategic Partners, for committing to take tinyML to the next Level, together
Executive Strategic Partners
Advancing AI research to make efficient AI ubiquitous

Power efficiency
- Model design, compression, quantization, algorithms, efficient hardware, software tool

Personalization
- Continuous learning, contextual, always-on, privacy-preserved, distributed learning

Efficient learning
- Robust learning through minimal data, unsupervised learning, on-device learning

Perception
- Object detection, speech recognition, contextual fusion

Reasoning
- Scene understanding, language understanding, behavior prediction

Action
- Reinforcement learning for decision making

A platform to scale AI across the industry
Accelerate Your Edge Compute

SYNTIANT

Making Edge AI A Reality

www.syntiant.com
Platinum Strategic Partner
DEPLOY VISION AI AT THE EDGE AT SCALE
Gold Strategic Partners
Build the Future of tinyML on ARM
EDGE IMPULSE

The Leading Development Platform for Edge ML

dgeimpulse.com
Driving decarbonization and digitalization. Together.

Infineon serving all target markets as Leader in Power Systems and IoT

www.infineon.com
NEUROMORPHIC INTELLIGENCE FOR THE SENSOR-EDGE
Renesas is enabling the next generation of AI-powered solutions that will revolutionize every industry sector.
STMicroelectronics provides extensive solutions to make tiny Machine Learning easy
ENGINEERING EXCEPTIONAL EXPERIENCES

We engineer exceptional experiences for consumers in the home, at work, in the car, or on the go.

www.synaptics.com
Silver Strategic Partners
Join Growing tinyML Communities:

tinyML - Enabling ultra-low Power ML at the Edge

The tinyML Community
https://www.linkedin.com/groups/13694488/

17.4k members in
49 Groups in 41 Countries

4k members
&
13k followers
Subscribe to tinyML YouTube Channel for updates and notifications (including this video)
www.youtube.com/tinyML
tinyML Asia
Technical Forum

November 16, 2023
Seoul, South Korea

Register now
https://www.tinyml.org/event/asia-2023/
2023 Edge AI Technology Report

The guide to understanding the state of the art in hardware & software in Edge AI.

https://www.wevolver.com/article/2023-edge-ai-technology-report
Reminders

Slides & Videos will be posted tomorrow

tinyml.org/forums  youtube.com/tinyml

Please use the Q&A window for your questions
Mohamed Shalan

Mohamed Shalan is the Head of Design and EDA at Efabless Corporation. Before his role with Efabless, Mohamed held various engineering positions at several organizations, including Mentor Graphics, Motorola SPS, and Mindspeed. Mohamed holds a Ph.D. degree in computer engineering from the Georgia Institute of Technology. His research interests are multifaceted, encompassing open-source EDA, hardware, and software codesign for embedded systems, with a strong emphasis on low-power computing. His contributions to these areas have resulted in over 40 peer-reviewed publications and three US patents.
Unlocking TinyML

A Cost-Efficient Approach to Custom Microcontroller Design for AI Applications
Microcontrollers

- It is estimated that around 300 billion microcontrollers are in the world today
- Around 38 billion units to be shipped in 2023 alone (estimated)
- Strong microcontroller growth in recent years was driven by IoT applications
- The current growth will be driven by TinyML
Are microcontrollers ready for TinyML wave?

But, microcontrollers are sub-optimal!
Desired functionality

```plaintext
total = 0
for i = 1 to N
    loop
        total += M[i]
    end loop
```
**Why Custom SoCs?**

- Optimized Performance
- Energy Efficiency
- High Integration ➔ Lower cost
- Protecting your IP
- Create the differentiator
- Cost Efficiency in the Long Run
- Controlling your supply chain
- …
Why not Custom SoCs?

- Cost, high NRE
- Foundry PDK Access
- IP Access
- Complexity
- High Risk
- …
At least these 6 things must exist to create useful chips

YOU CAN’T BUILD A USEFUL CHIP
Partial solutions don’t work

STILL CAN’T BUILD A USEFUL CHIP
Every design entity needs to establish independent business and contractual relationships with multiple IP providers, EDA vendors, and foundries.

TODAY’S APPROACH TO CUSTOM SILICON
Simplifying Chip Creation and Opening it to Everyone
The largest community of chip creators

Connect

Create

Collaborate

Design, manufacture and test your chips for under $10K.

Users and experts co-design custom chips for smart products.
Complete & Path from Design to Validation

1. DESIGN

2. INTEGRATE

3. SUBMIT

4. FABRICATE

5. TEST/Validate

OS or Proprietary EDA Digital & Analog
Start from the 18th floor to reach the 20th

Build on existing foundational work by others

You only need to know your design … or your code

User’s Area
10 mm²
(2.92mm x 3.52mm)

+ 

Your Design

CARAVEL + Your Design

Plug & Play Dev Board
Caravel SoC Platform

User's Project
~10 mm²
(2.92mm x 3.52mm)

https://github.com/efabless/caravel

Uniform Open Source File Structure to ease reuse & modifications

VexRISCV OpenRAM OpenROAD OpenLane
LOW COMPLEXITY

IP Development
Digital & low frequency analog
Enabling larger designer base

HIGH COMPLEXITY

IP Development
Complete Custom ASIC
Analog & Digital
Expert designer base

One Size Fits All
Automate code-to-chip like a **GNU software compiler** - with trade-offs in area and performance.

It opens the door for software developers to generate hardware. That’s at least a 1000x more potential designers!
A library of IP blocks

Open Source IP

Obfuscated Proprietary IP

- Silicon proven / verified functions
- Highly leveraged known proven IP blocks
- Scope of customization is constrained
- Standard IP packaging to enable reuse
Design using SkyWater SKY130 process + std cells + IO cells

Bring your Own EDA, use Open Source Flows or Use EF Cloud Synopsys EDA

Start from the Caravel Harness - book your slot for $200

You *choose your licensing terms* for your design - by default it’s *proprietary*

Design Area (10mm$^2$ or 15mm$^2$) is not just silicon area - *It is a framed house with plumbing and electricity - just bring your design!*

Cycle Time 95 days +/- depending on the package choice

<table>
<thead>
<tr>
<th>Rapid Prototyping</th>
<th>$9,750</th>
<th>100 QFN</th>
<th>parts + dev boards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Volume Production</td>
<td>$20,000</td>
<td>1000 QFN</td>
<td>parts + dev boards</td>
</tr>
</tbody>
</table>
10,000 community members
1,000 designs
500 chips
2 years!
### Selected Open Source IP Blocks

- A pseudo random number generator for critical real-time processors.
- A General Purpose Bandgap generating constant voltage at output, independent of Temp and Supply variations.
- Convolutional Neural Network Accelerator on a wishbone slave for Raven Core in Caravel SoC.
- Maverick 603 Radio
- Chaos automaton
- Arduino pin compatible Single RISCV 32 Bit core Project
- HSV to RGB color conversion accelerator
- CMOS Bandgap
- USB for RISC-V microcontroller
- Analog Spiking Circuit and 10-bit DAC
- Auditory perception acoustic front end
- GPS Baseband
- 1V8 LDO
- NAND Flash

### Select Open Source SoCs

- Sleep Apnea Detection System
- Electro Mechanical Water Quality Monitoring
- Influenza detector
- Image Detection at Edge of Neural Networks
- Satellite Radio
- Epileptic Seizure Detection
- LED Lighting for Bangladesh Solar Home System
- Nanopore DNA Sequencing
- Smart Garden
- Industrial Motor Controller
- Reconfigurable Flight Controller SoC for UAVs
- TinyML Image Detection at Edge with DNN
- Donkey Kong Bongo PS2 Keyboard
**2021 IEEE SSCS Chipathon**

<table>
<thead>
<tr>
<th>Function</th>
<th>Team</th>
<th>Chip URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 5G bidirectional amplifier</td>
<td>Pakistan3 (FAST National University)</td>
<td><a href="https://efabless.com/projects/560">https://efabless.com/projects/560</a></td>
</tr>
<tr>
<td>2 Wireless power transfer unit</td>
<td>Pakistan2 (FAST National University)</td>
<td></td>
</tr>
<tr>
<td>3 Variable precision fused multiply-add unit</td>
<td>Pakistan1 (FAST National University)</td>
<td></td>
</tr>
<tr>
<td>4 Oscillator-based LVDT readout</td>
<td>India2 (Anna University)</td>
<td></td>
</tr>
<tr>
<td>5 Temperature sensor</td>
<td>India1 (Anna University)</td>
<td></td>
</tr>
<tr>
<td>6 GPS baseband engine</td>
<td>India3 (Anna University)</td>
<td></td>
</tr>
<tr>
<td>7 Ultra-low-power analog front-end for bio signals</td>
<td>Brazil2 (U. Federal de Santa Catarina)</td>
<td></td>
</tr>
<tr>
<td>8 TIA for quantum photonics interface</td>
<td>USA4 (University of Virginia)</td>
<td></td>
</tr>
<tr>
<td>9 Bandgap reference</td>
<td>Egypt (Cairo University)</td>
<td></td>
</tr>
<tr>
<td>10 Neural network for sleep apnea detection</td>
<td>USA2 (University of Missouri)</td>
<td></td>
</tr>
<tr>
<td>11 SONAR processing unit</td>
<td>Chile (University of the Bio-Bio)</td>
<td></td>
</tr>
</tbody>
</table>

*Link to Article*  [SSCS Magazine Article - NOV 2021](#)

**Paid runs via Efabless chipIgnite (130 nm SkyWater)**

**All designs are open source**

© 2023 EFABLESS CORPORATION

Made possible with Efabless’ chipIgnite
<table>
<thead>
<tr>
<th>Function</th>
<th>Team</th>
<th>Chip URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Spatial Sigma-Delta ADC</td>
<td>Pakistan1†(FAST National University)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1486</td>
</tr>
<tr>
<td>2 On-Chip DCDC Converter with Fast Transient Response</td>
<td>Pakistan4†(FAST National University)</td>
<td></td>
</tr>
<tr>
<td>3 Matrix Multiplier for AI at the Edge</td>
<td>Pakistan7†(FAST National University)</td>
<td></td>
</tr>
<tr>
<td>4 Encrypted LSB Steganography with AES Accelerator</td>
<td>Pakistan2†(FAST National University)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1443</td>
</tr>
<tr>
<td>5 CMOS Bandgap Reference</td>
<td>Pakistan3†(FAST National University)</td>
<td></td>
</tr>
<tr>
<td>6 Self-Interference Cancellation LNA</td>
<td>Pakistan4†(FAST National University)</td>
<td></td>
</tr>
<tr>
<td>7 Sub-Sampling PLL for SerDes Applications</td>
<td>Austria (Johannes Kepler Univ., Linz)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1431</td>
</tr>
<tr>
<td>8 60 GHz Demonstrator Chip</td>
<td>Brazil (University of São Paulo)</td>
<td></td>
</tr>
<tr>
<td>9 Low-Power 10-bit SAR ADC</td>
<td>USA1 (University of Alabama &amp; MIT Lincoln Lab)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1431</td>
</tr>
<tr>
<td>10 Boost Converter for Battery-Powered IoT Applications</td>
<td>Greece (Aristotle University of Thessaloniki)</td>
<td></td>
</tr>
<tr>
<td>11 Radiation-Hardened ALU</td>
<td>USA2 (North Carolina A&amp;T State University)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1457</td>
</tr>
<tr>
<td>12 DC-DC Buck Converter for CubeSat</td>
<td>Chile1†/Argentina2†/Uruguay3†</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1427</td>
</tr>
<tr>
<td>13 Electrochemical Water Quality Monitoring</td>
<td>USA5 (University of Tennessee)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1469</td>
</tr>
<tr>
<td>14 Mix-Pix - A Mixed-Signal Circuit for Smart Imaging</td>
<td>Chile (Universidad del Bio-Bio)</td>
<td><a href="https://platform.efabless.co">https://platform.efabless.co</a> m/projects/1494</td>
</tr>
<tr>
<td>Project Name</td>
<td>URL</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------------</td>
<td>------------------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>caravel_fulgor_opamp</td>
<td><a href="https://efabless.com">efabless.com</a></td>
<td>Operational amplifier (opamp) based on the Miller topology designed in Skywater SKY130 CMOS process.</td>
</tr>
<tr>
<td>SHA1 engine</td>
<td><a href="https://github.com/kzimny">Krzysztof Zimny</a></td>
<td>The SHA1 engine, while not the most secure nowadays is still used by git commits and TPM PCR..</td>
</tr>
<tr>
<td>Caravel-SOFA-HD</td>
<td><a href="https://efabless.com">efabless.com</a></td>
<td>Xifan Tang</td>
</tr>
<tr>
<td>FWPayload</td>
<td>[Matthew Ballance](<a href="https://github.com/mm">https://github.com/mm</a> Ballance)</td>
<td>A simple RISC-V core+peripherals subsystem for the Google-sponsored Open MPW shuttles for SKY130.</td>
</tr>
<tr>
<td>Caravel_Astria_Testchip</td>
<td><a href="https://efabless.com">efabless.com</a></td>
<td>Astrid Nur Irlansyah</td>
</tr>
<tr>
<td>HS32Core</td>
<td><a href="https://efabless.com">efabless.com</a></td>
<td>Kevin Mack Baragona</td>
</tr>
</tbody>
</table>
But, Where is TinyML?
Cheetah SoC

- Targets applications that involve a trained ML models to process low speed sensor data/signal including audio.
- Has ML and Security accelerators
Cheetah SoC Iterations

Cheetah SoC V1
Taped out: Sept. 23
Caravel

Cheetah SoC V2
Tape out: Nov. 23
Open Frame
More Information about Efabless and chipIgnite

https://efabless.com/

Join the Open Source Silicon Community

https://open-source-silicon.dev/
Thank you!
Copyright Notice

This multimedia file is copyright © 2023 by tinyML Foundation. All rights reserved. It may not be duplicated or distributed in any form without prior written approval.

tinyML® is a registered trademark of the tinyML Foundation.

www.tinyml.org
Copyright Notice

This presentation in this publication was presented as a tinyML® Talks webcast. The content reflects the opinion of the author(s) and their respective companies. The inclusion of presentations in this publication does not constitute an endorsement by tinyML Foundation or the sponsors.

There is no copyright protection claimed by this publication. However, each presentation is the work of the authors and their respective companies and may contain copyrighted material. As such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

tinyML is a registered trademark of the tinyML Foundation.

www.tinyml.org